Microcontroller Based PWM UPS

by

Azher Mehboob Rana

A Thesis Presented to the

FACULTY OF THE COLLEGE OF GRADUATE STUDIES

KING FAHD UNIVERSITY OF PETROLEUM & MINERALS

DHAHRAN, SAUDI ARABIA

In Partial Fulfillment of the
Requirements for the Degree of

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In

ELECTRICAL ENGINEERING

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King Fahd University of Petroleum and Minerals (Saudi Arabia), 1992

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This thesis, written by

Azher Mehboob Rana

under the direction of his thesis committee, and approved by all the members, has been presented to and accepted by the Dean, College of Graduate Studies, in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

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Date : Aug. 3rd, 1992

Dedicated to

My Parents

Acknowledgment

I wish to thank my thesis committee chairman Dr. Ibrahim El-Amin for his guidance, and committee members Dr. A, K. Al-Ali and Dr. G. F. Beckhoff for their support.

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Abstract

Name: Azher Mehboob Rana

Title: Microcontroller Based Pulse Width Modulated Uninterruptible Power Sytem

Major Field: Electrical Engineering

Date of Degree: July 1992

The thesis describes the simulation and implementation of a microcontroller based single phase pulse width modulated uninterruptible power system employing ultrasonic switching frequencies. VDMOS transistors have been used as switching elements. PSPICE model for a VDMOS has been developed and added to the library. A unique method for the simulation of regular sampled PWM and digital feedback has been tried. The use of microcontroller in the UPS makes it more flexible and consistent. Ultrasonic carrier frequencies are employed, this reduces the size of the filter elements. Input transformer is eliminated by the use of doubler and chopper section. High voltage battery eliminates the need for a step up output transformer. This makes the overall design compact, efficient and reliable. Digital simulation of the complete UPS circuit has been performed. Laboratory implementation has been carried out and the results are presented.

Master of Science Degree

King Fahd University of Petroleum and Minerals

Dhahran, Saudi Arabia

July 1992

خلاصـــــة

الأســـم : أظهر محبوب رانـا

العنوان : نظام طاقة غير منقطع معتمد على طريقة تضمين عرض النبضه باستعمال المتحكمات الدقيقه (الميكروكنترولر) .

التخصص : الهندسة الكهربائيـــة

التاريخ : تموز ١٩٩٢م ــ محرم ١٤١٣هـ هـ

تصف رسالة الماجسيتر هذه محاكاة وتنفيذ نظام طاقة غير منقطع معتمد على طريقة تضمين عرض النبضه باستعمال المتحكم الدقيق (الميكروكنترولر) وبالاستعانة بالترددات فوق الصوتية ، وقد استعملت الترانزستـــورات VDMOS كعناصر تبديل . وتم بناء نموذج للترانزستور VDMOS وأضيف الى مكتبة البرنامج PSPICE . كما تم استحداث طريقة لمحاكاة عملية أخذ عينات تضمين عرض النبضه وعملية التغذية الرجعية الرقمية . ان استعمال المتحكمات الرقمية فى أنظمة الطاقة غير المنقطعه يعطى هذه الأنظمة مرونه أكبر وتوافقا أكثر . ومن جهة أخرى فان استعمال الترددات فوق الصوتية يؤدى الى صغر حجم عنصر التنقية . وقد تمت الاستعاضة عن محول المدخل باستعمال مضاعفات ومقسمات الجهد . كما تمت اللاستعاضة عن محول المخرج باستعمال بطاريات ذات جهد عال . كل ماتقدم ساهم فى جعل التصميم أقل حجما وأكثر كفاءة وفعالية . وقد تمت محاكاة النظام بأكمله ، كما تم بناء هذا النظام فى المعمل ، وأخذت النتائج والقرارات .

درجة الماجستير فى العلوم

جامعة الملك فهد للبترول والمعادن

المملكة العربية السعوديـــــــــة

الظهـــران

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Chapter 1

INTRODUCTION

With the increasing use of sophisticated electronic equipment, users have become more aware of the common problems caused by the imperfections of the main power supply. These problems include over/under voltage transients, voltage sags, spikes noise, frequency aberrations, loss of few cycles and even complete mains failure, some or all of which can cause the malfunctioning of on line electronic equipment. An AT&T Bell Laboratories study shows that a typical site in the U.S experiences *135 commercial ac-power disturbances a year* [1].

The source of the spikes and noise may be other equipment working in the same area. Thunder storms/seismic disturbances can also generate noise which can cause interruptions in the supply lines. The aberrations in the voltage and frequency could be due to stretched mains lines particularly during the peak hours. Various types of devices and equipment such as isolation transformers constant voltage regulators, ferro resonant transformers, line conditioners etc. are usually used to minimize or eliminate mains disturbances . The above mentioned devices can reduce transients,

spikes, and can absorb high or low voltages with varied degree of success. However, none of them can regulate the voltage under widely varying load conditions or regulate/control frequency at all and are totally unable to generate missing cycles. To provide complete protection against all the irregularities and disturbances which can be the cause of malfunctioning of the critical loads, the user must turn to the only form of power conditioning devices capable of meeting these requirements, *i.e. the Uninterruptible Power Supply (UPS).*

1.1 Literature Survey

During the last decade UPS systems have undergone several major changes mainly due to benefit from the developments in power semiconductor devices , microprocessors, maintenance free sealed lead acid batteries and improvements in control techniques. Thus it has become one of the *fastest growing fields of power electronics.* UPS systems could be categorized into two types, namely, rotary and static UPS systems. The merits and demerits of both types are described and special emphasis is placed on recent developments in UPS systems such as those employing improved topologies, new devices and control techniques implemented with microprocessors. These new topologies consist of low impedance rotary UPS, PWM UPS, triport UPS, and hybrid UPS systems [2].

Due to advancement in power switching device technologies and refinements in PWM techniques, the PWM UPS has become one of the most promising fields in power electronics engineering. The PWM inverter and its control circuits are the most sophisticated part of a UPS system and its design determines the reliability, flexibility

and the quality of the output waveform. The main aim of the PWM inverter are to eliminate as many low order harmonics as possible at the switching stage and to effect control over voltage and frequency with a single power stage [3].

Improvements in digital VLSI/microprocessor technologies have resulted in their frequent use in many fields of power electronics. The immediate advantages of using digital VLSI/microprocessor controlled systems are that they increase the *flexibility and consistency* of the controller. The controller is then devoid of inherent drawbacks of analogue controllers such as those related to component aging and temperature drift. PWM is the only method that can allow the output to be *precisely controlled on a sub-cycle basis.* Most other methods are only able to regulate the output voltage based on the average value of the phases [4]. The microprocessor controlled implementation of PWM techniques at switching frequencies up to few kHz have received considerable attention. These PWM generators suffer from some inherent problems associated with microprocessors. These include interrupt delays which introduces a certain degree of distortion in the output waveform. Little attention has been given to microprocessor controlled PWM inverters employing *ultrasonic carrier frequencies.* However, such inverters offer more flexibility in design and can result in a *reduction of hardware components* and *increase in the reliability.*

The main objectives of this thesis are to implement the regular sampled PWM strategies employing a 20 kHz carrier frequency using a microprocessor. The inverter section uses VDMOS transistors The performance of these is compared with ordinary MOS transistors. In addition all the control functions required by such an

inverter will be implemented by a single microprocessor.

1.2 Organization of the Thesis

The thesis describes the simulation of a microprocessor controlled single- phase pulse width modulated (PWM) UPS employing a switching frequency of 20 kHz. A block diagram of a microprocessor controlled UPS system is shown in Fig 1.1. Single edge regular sampled PWM strategies have been used to generate PWM pulses for the inverter. A digital control is utilized to regulate the output voltages.

Chapter Two gives description of the various UPS systems and discusses their advantages and disadvantages. The different kind of inverters being used in UPS applications are discussed so as to provide the necessary background to the understanding of various UPS systems. A comparison of the thesis approach to conventional approach is presented.

Chapter Three discusses the sinusoidal PWM strategies available in the literature. The problems encountered in generating PWM pulses using high frequency are discussed followed by a discussion on single edge, double edge synchronous and asynchronous PWM. The importance of using a 20 kHz carrier signal in UPS applications are discussed. A regular-sampled symmetric PWM strategy is selected for implementation because of its simplicity. Two equations to achieve single-edge and double edge modulations are derived. Different methods of calculating the Look-Up Table data (LUT) are presented.

Chapter Four is mainly concerned with the design and simulation of the different sections of the UPS. VDMOS model for computer aided design has been developed. This models will be incorporated in the PSPICE package which is to be used for the simulation studies. The need for high speed gate driver is discussed, and a model for high speed gate driver has been simulated. The doubler and battery charger section has been designed and simulated. Simulation of PWM has been carried out.

Chapter Five deals with the laboratory implementation of various building blocks of the UPS. PWM is generated using analog techniques. Doubler, chopper, inverter, and filter section were built in the laboratory and implementation results are presented. The unique method of digital feed back simulation has been discussed and the results are shown. Various methods for monitoring and diagnostics are described.

Chapter Six presents general conclusions and some suggestions for future work are also made.

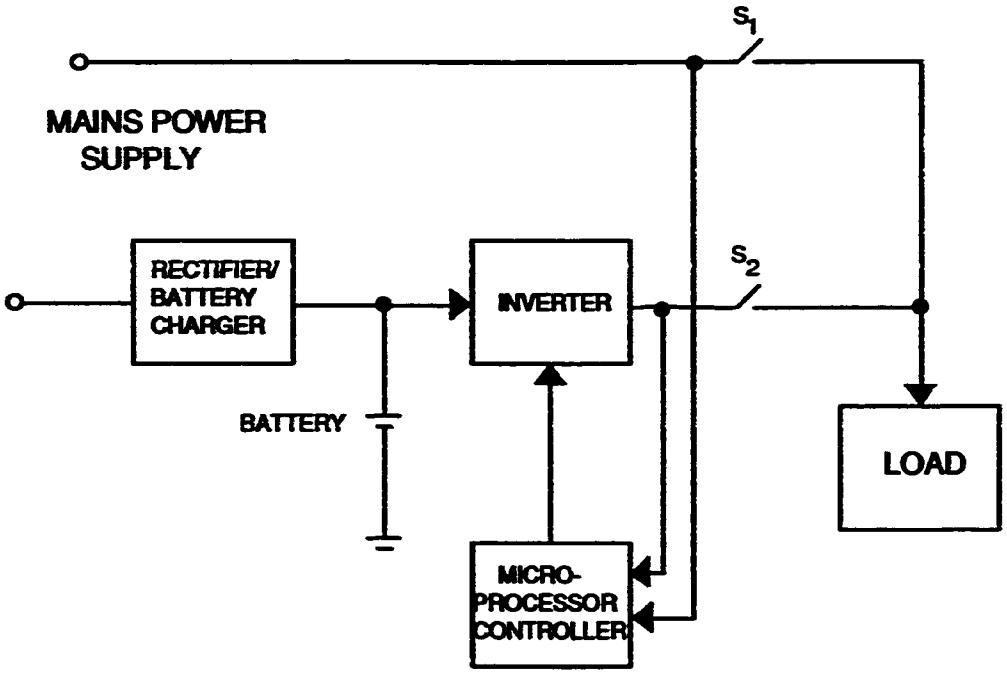


Figure 1.1: A microprocessor controlled UPS system

Chapter 2

UNINTERRUPTABLE POWER SYSTEMS

In this section Uninterruptible Power Systems are described with their merits and demerits. Static inverters using magnetic and electronic techniques are discussed in detail to highlight their characteristics. In addition the comparison of the approach developed in the thesis with the conventional approach is presented. The advantages of the proposed design are discussed.

Due to the increase in the use of computer systems, process control systems, automatic production lines, telephone exchanges, communications networks etc., the demand for Uninterruptible Power Supplies (UPSs) is increasing. UPSs are the *only form of power conditioning devices* available that provide protection against all the irregularities and disturbances which can be the cause of malfunctioning of the critical loads. In general there are two distinct methods by which a UPS system can be connected to a critical load [4]. The block diagrams of both the configurations

are shown in the figure 2.1 and 2.2. These are categorized into *on-line and standby UPS systems.* Both configurations use the same number of components but differ in the way the components are connected to the critical load. When the on-line system is operating, the system protects the load from all kinds of aberrations in the mains supply. In the event of mains failure, the system supplies uninterrupted power from the batteries since those are permanently at the input of the inverter. In contrast to the on-line system, the standby system only comes into operation when the mains failure is detected, whereas the load is normally supplied directly or through a line conditioner by the mains.

The standby UPS has the main advantage over the on-line UPS of a *higher operating efficiency* since it does not have to supply power at all times. The standby UPS therefore has lower running cost but the on-line UPS provides more *precise voltage and stable frequency controls.* The standby UPS cannot be used in those applications where loads are sensitive to frequency variations because the frequency of the mains power supply cannot be guaranteed. The *on-line UPS systems are therefore preferred* due to their higher quality of power delivery and reliability.

2.1 Rotary UPS

A standard rotary UPS is shown in Figure 2.3. Its DC/AC converter consists of *DC motor driving an AC alternator* with or without a flywheel. Stable frequency operation is achieved by regulating the output speed of the DC motor and the output voltage of alternator is regulated by the use of an automatic voltage regulator. The output voltage waveform and the frequency may be synchronized with that of the

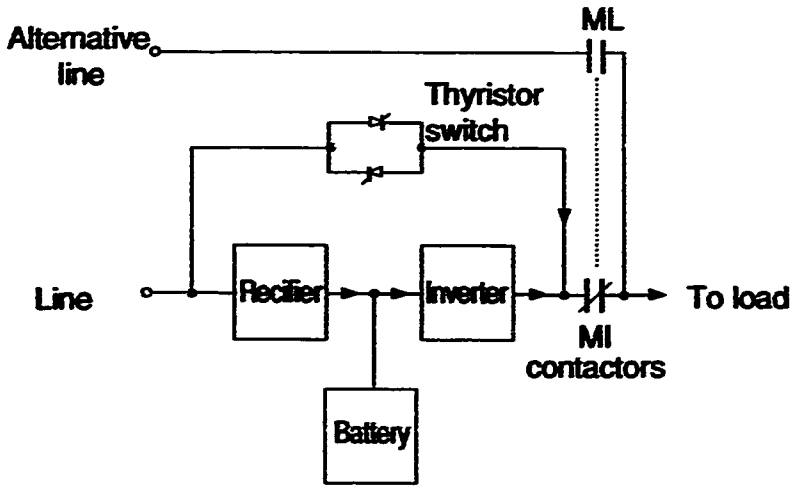


Figure 2.1: On line UPS

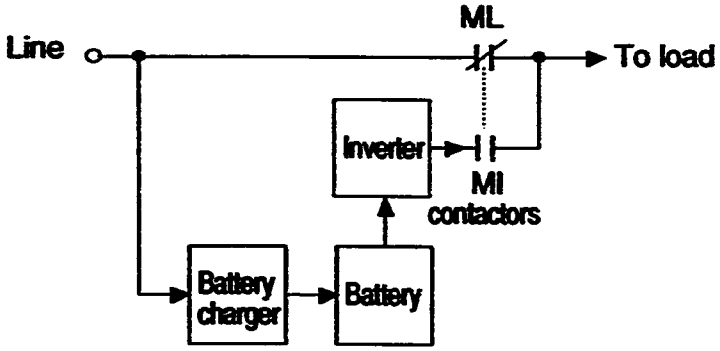


Figure 2.2: Standby UPS system

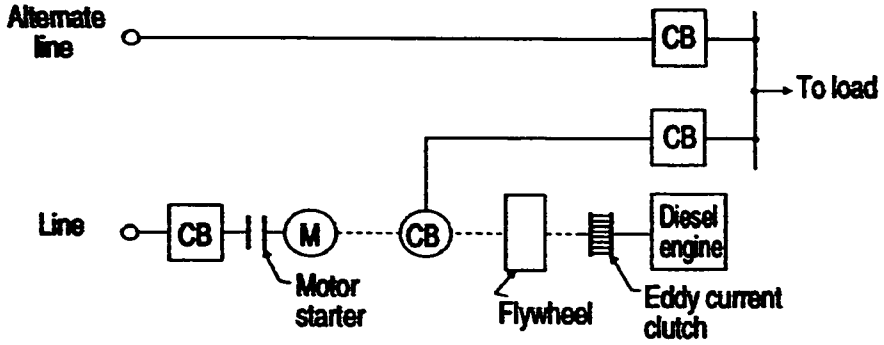


Figure 2.3: Rotary UPS

mains.

2.2 Static UPS

In the static UPS system, a static *inverter utilizing power semiconductor devices* is used instead of a motor and alternator. The inverter converts the DC input into AC voltage waverforms by one of the many available switching techniques, the most common of which are *pulse width modulation*, *phase shifting techniques*, *quasi-square wave techniques* and *magnetic techniques*. The output voltage generated by these inverters generally requires filtering to reduce harmonics and to make the waveform sinusoidal.

2.3 Components of the UPS System

A UPS system may consist of four major components:

- Rectifier/battery charger
- Bank of batteries
- DC to AC inverter
- Control circuitry

The *rectifier and inverter units* are employed in many combinations to supply a critical load; singly, in parallel, or with a switch backed up by an engine generator set. The particular combination selected is determined by the magnitude of the load power, the pattern of anticipated AC line interruptions and the sensitivity and critical nature of the load.

2.3.1 Batteries

A bank of batteries is invariably used in every UPS system as a reserve DC power source. The batteries are normally a secondary type which means these are electrically rechargeable. Only in a few low power applications are primary type batteries used, which are then discarded after use. The required DC voltage and current ratings are obtained by connecting the batteries in series and parallel combinations. The batteries provide DC input to the inverter when rectifier output voltage drops below the acceptable range.

In choosing a battery for use in UPS applications, several important aspects should be taken into account [5]. These include the *rate of discharge* of current, the necessary *backup time* and the acceptable *voltage variations.* In addition, reliability environment, space, weight, and cost must also be taken into account before making a decision about type of battery to be employed. The battery size determines (ampere- hour) the time during which power can be drawn from the batteries.

For UPS applications, the choice is between two basic battery types namely the wet and gelled cell batteries. The wet cell batteries are available in two types; lead acid and nickel cadmium batteries.

Lead-acid batteries are most commonly used due to their low cost, reliability and excellent performance characteristics in float applications. The most common types of lead acid batteries are the lead-calcium and lead-antimony batteries. All wet batteries under certain conditions can generate noxious gases therefore, sufficient ventilation arrangements should be made.

Sealed batteries are available in both gelled/absorbed electrolyte constructions but *nickel cadmium* are more commonly used. These are alkaline in contrast as compared to lead-acid batteries. Unlike the lead acid batteries the measurements of specific gravity do not provide an indication of state of charge in nickel cadmium batteries. Nickel cadmium batteries have long life spans (10 years). Sealed batteries are generally considered expensive for high power UPS systems but these are widely used in small portable UPS systems. Also these are preferred where improved low temperature operation and/or extremely short duration/high rate of discharge currents are required.

2.3.2 Rectifier/Battery Charger

For on-line UPS systems, the rectifier/battery chargers are used to provide power to the load and charging current required by the batteries. The rectifier/charger unit regulates the DC voltage by varying the firing angle of the Silicon Controlled Rectifiers (SCRs). For single phase they employ 2 pulses, in three phase circuit 6 pulses are used, additional pulses 12 or 24 may be achieved by creating additional phases in a transformer for the improvement of the input power factor and the current waveforms at the higher ratings. For low power ratings the above scheme is not cost effective instead, rectifiers along with chopper can be used. The output filtering can be reduced significantly, and input power factor improved considerably by utilizing PWM schemes for the charger section [2].

Since the standby UPS systems are usually used for small power applications and do not supply power in normal mode, only a battery charger is required to supply

the charging current or trickle charging current to compensate the internal losses of the batteries. On-line UPSs are always getting power from the batteries so the charger should be able to supply the total required current, thus so the charger section becomes bigger and bulky in on-line UPS systems.

2.3.3 Inverters

The main function of an inverter in conjunction with an output filter is to convert DC into AC voltage. The critical load is normally supplied by an inverter, the *design of which determines the quality of the AC power delivered to the load.* Thus, the inverter together with its control circuit should be designed to fulfil the following primary requirements [2].

1. The inverter should be capable of generating a good quality output waveform and the total harmonic distortion should be less than the 5 percent of the output which is acceptable to most of the critical loads.

2. The output voltage regulation should be within 5 percent (typically 1 percent) with fully charged/discharged state of the batteries.

3. The transient response of the inverter to the step load change from no load to full load should be less than 5 cycles (typically less than one cycle) with voltage exclusion less than 15 percent.

4. The output frequency must be stable within $\pm$ 0.005 percent (typically $\pm$ 0.001 percent) and the rate of change of frequency should not be more than 0.5 Hz per second.

5. The control circuit for operating the static switch must be capable of detecting any abnormalities in the output frequency and voltage (from the preset limits) in one second (typically after one period) and after one cycle (typically instantaneously) respectively.

6. The output waveform should be capable of being synchronized with the mains supply within the preset limits.

Although several kinds of inverters exist in the literature, each meets the above requirements with varied degree of success. All inverters use semiconductor devices as switching components but differ in the way the output voltage regulation is achieved. Several techniques are available to regulate the output voltage. These can be categorized into two groups namely magnetic techniques and electronic techniques.

Inverters Using Magnetic Techniques

The magnetic techniques are those which rely mainly on the magnetic saturation of the output transformer or output inductors for the required output voltage [6].

The UPS employing these inverters are rugged, reliable and require simple control circuits. Since these systems usually work as standby power sources, their efficiencies are considered reasonable. These systems always experience considerable overshoot upon load removal and considerable under voltage upon addition of load because of the energy stored in the magnetic components. Since these systems use low frequency tuned filters and 50/60 Hz transformers, they are thought to be noisy and heavy.

Inverters Using Electronic Techniques

The inverters use power conversion techniques such as pulse width control and feedback control circuits to synthesize the output waveforms. These inverters can be categorized into the following types; pulse width controlled inverter, stepped wave inverter and sinusoidal pulse width modulated inverter [5]. The methods to control the inverter output are discussed below.

Pulse width control: In this method the output voltage is controlled by varying the width of the output pulses, as shown in the fig 2.4. Fourier analysis of such a waveform gives the rms value of the nth coefficient as

$$\frac{V_{rms(n)}}{V_B} = \left[\frac{2\sqrt{2}}{n\pi} cosnD\right] \times 100 \tag{2.1}$$

Where V_B is the peak value of the square wave D is the delay time, and n is the number of the harmonic. the total rms voltage of the waveform including all the harmonics is

$$\frac{V_{rms(T)}}{V_B} = \left[1 - \frac{2D}{\pi}\right]^{1/2} \times 100 \tag{2.2}$$

The output waveform essentially requires large filtering components to decrease the harmonic content to an acceptable level.

Another approach is multiple pulse width modulation. Harmonic content can be significantly reduced by using several pulses in each half cycle of the output voltage [7]. This type of modulation is also known as uniform pulse width modulation.

Stepped Wave Inverters: The stepped wave inverters either change transformer taps or add schematically the output waveforms of several single-phase inverters with shifted controls to achieve the resultant stepped waveform which should closely approximate a sine waveform [5].

Stepped wave inverters are usually employed in larger three phase installations, where several inverters are run in parallel but phase shifted. The output of the inverters are summed by a transformer to produce a stepped waveform with reduced harmonic content. The same effect can be obtained by using a tapped supply as shown in the figure 2.5.

Sinusoidal Pulse Width Modulated Inverters: The sinusoidal PWM inverters synthesize the output waveform by switching the power devices at a higher frequency than the desired fundamental frequency. The aim of such inverters are to minimize as many low order harmonics as possible and also to effect control over voltage and frequency with a single switching stage[Bowes-75].

Inverters using these strategies are switched at the intersection of a triangular carrier and sine wave modulating signal as shown in the figure 2.6. Commonly used strategies are the natural sampling strategy and regular sampled switching strategy. Voltage control is usually achieved by varying the amplitude of the sine reference waveform. The harmonic distortion in the output waveform occurs at the carrier frequency and its side bands and multiples of the carrier frequency. The magnitude of the distortion decreases with an increase in the modulation index and is therefore lowest at 100 percent modulation. These strategies provide inherent voltage control and lend themselves to easy imple-

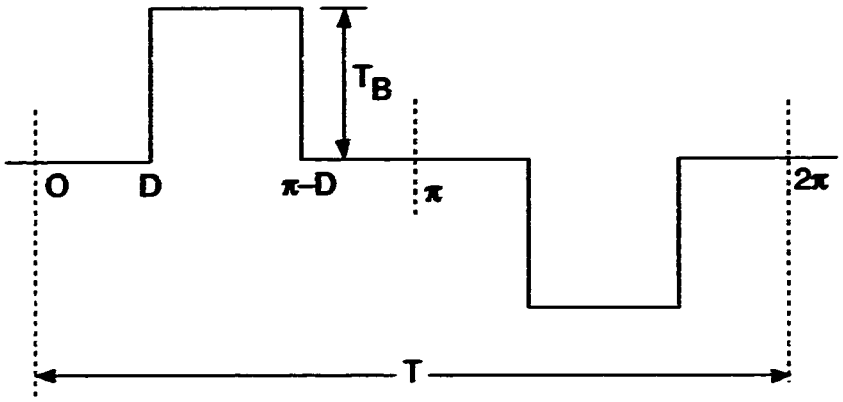


Figure 2.4: Single pulse width modulation

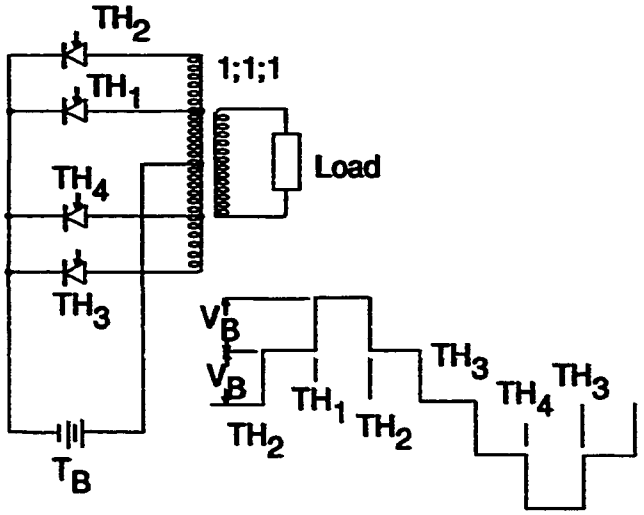


Figure 2.5: Wave form synthesis using a tapped supply

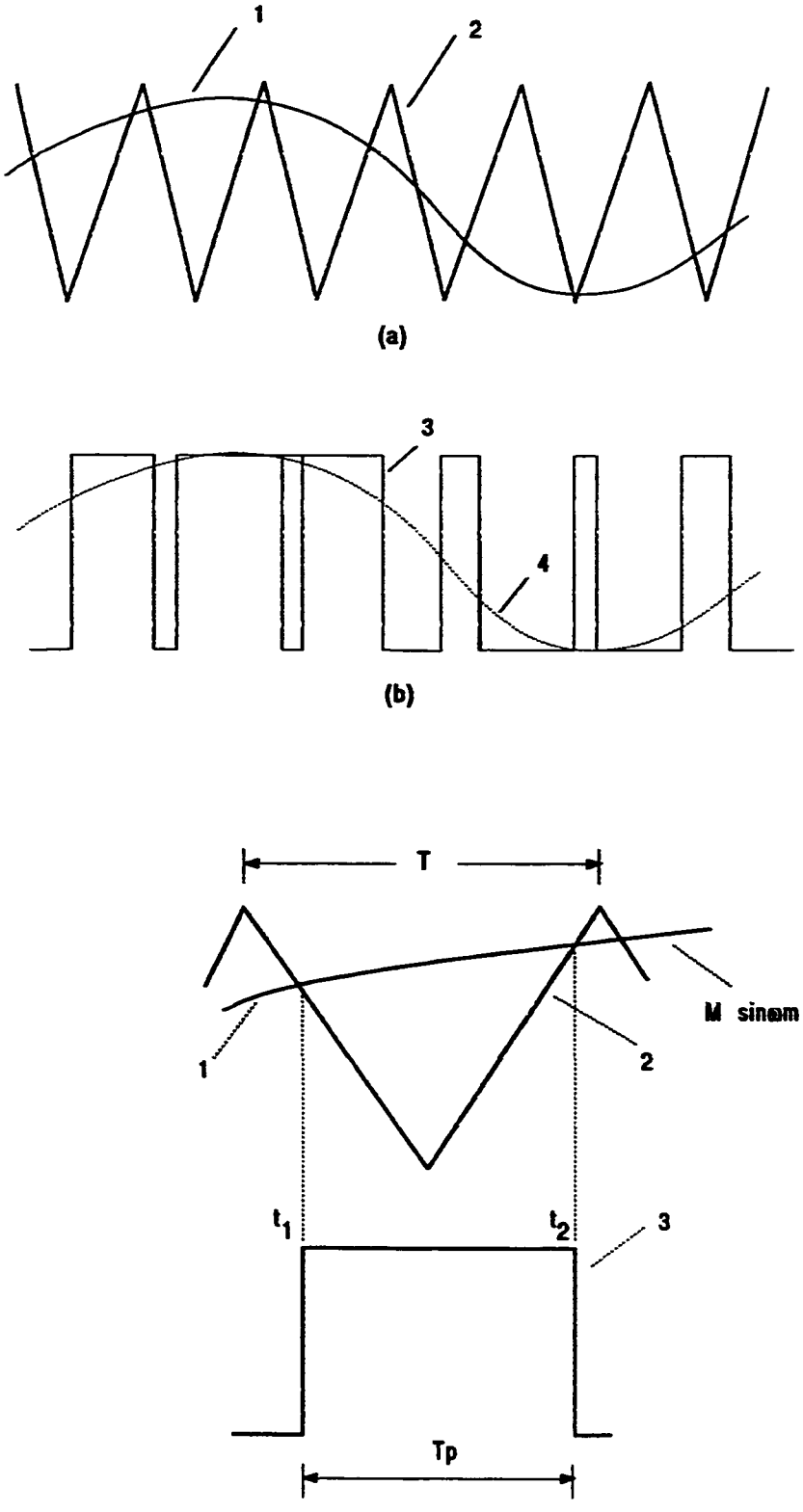


Figure 2.6: Sinusoidal pulse width modulation

mentation by a microprocessor controlled PWM generator.

Recently available UPS systems use PWM inverters with thyristors, GTOs and bipolar transistors. Although thyristors have excellent power handling capabilities, their slow switching speeds and the accompanied commutation circuitry and associated switching losses restrict the switching frequencies up to few kHz. GTO PWM inverters eliminate the commutation circuit required by conventional thyristors but at the expense of sophisticated gate drive circuit and protection scheme.

Advances in power MOSFET and bipolar transistor technologies allow the switching frequencies of low and medium power inverters to be increased up to several tens of kHz. By using a high switching frequency, the least desirable harmonics are well separated from the fundamental component, thereby permitting the use of the simplest PWM strategy. AC filtering can then be accomplished with a simple two elements LC low pass filter instead of the multicomponent tuned networks used in low frequency inverters. The use of switching frequencies above the audio range allow inverters to be realized without acoustic noise. MOSFETs are being preferred foe use in inverters because of their simple gate drive circuit requirements, fast switching speeds ease of paralleling operation and wide operating area[khan-88].

2.4 Power Semiconductor Devices

The present range of power semiconductor devices available for application in power conversion equipment has developed from the original range of diodes and conventional thyristors into a large family which now includes gate turn-off thyristors, static induction transistors, static induction thyristors, bipolar power transistors, IGBTs, and power MOSFETs [8]. Some of the above mentioned devices either have a limited field of applications or are still only available in small sizes and quantities and have not yet reached such a stage of development that they can be regarded as established standard devices. It is therefore decided to discuss popular devices used in UPS inverter applications. These are the conventional thyristor, the GTO, the bipolar power transistor and the power MOSFET. Newly introduced VDMOS will also be discussed.

Traditionally, conventional thyristors are used in inverter applications due to their low cost and excellent power handling capabilities. However, despite the advantages of requiring simple drive circuitry to turn the device on, they require auxiliary circuits for turn-off. This may consist of commutating LC network/ and an additional auxiliary thyristor. Furthermore, these devices have a stringent requirements regarding the rate of rise of on-state current, dI/dt. If the rate of rise of current is too high, an area around the gate will be overheated due to the initial on-state current concentration in that area and, consequently the device may be damaged, On the other hand a high rate of rise of voltage may cause false triggering. To keep dI/dt and dV/dt within the prescribed limits, the thyristor must be series connected with and inductance and in parallel with an RC elements , called the snubber circuit.

Turn-off commutation circuit losses increase with frequency and are usually significant at high switching frequencies. Also, due to their slow switching times and need to allow sufficient time to reset the turn-off snubber, conventional thyristors are not recommended for use in PWM inverters at high switching frequencies. The turn-off commutation circuits required by conventional thyristors can be eliminated by replacing the thyristor with totally gate controlled devices such as the GTO thyristor, bipolar transistors and power MOSFET. The GTO thyristor has similar characteristics to those of the transistors are widely used in Variable Speed Drives(VSDs) and UPS applications. Since these devices do not require complex commutation circuitry, the resulting inverter should be smaller and lighter and will produce less acoustic noise than its conventional thyristor counterpart.

GTOs and bipolar transistors have almost similar turn-on drive requirement as high pulse current is required for fast turn-on followed by continuous on-drive, especially in the case of the bipolar transistor. Also, in general, both devices require large reverse currents for fast and reliable turn-off, although the transistor will turn off without reverse bias current but its turn-off will be slowed down. In the off state both devices require benefit from reverse biased control junctions since it increases its noise immunity.

The GTO thyristors suffer from a long storage time and current fall time as well as tail currents. In addition, to achieve shorter turn-off times the turn off gain must decrease and may reach unity. The GTO also suffers from a relatively low

dV/dt ratings which necessitates rather large snubber capacitors. Unless loss less snubbers are used, the snubber capacitor loss which is dissipated in the device at turn-on, becomes large. That is why the use of GTO thyristors have been restricted to low switching frequency applications¡5kHz). The bipolar power transistor can be operated at higher switching frequencies at maximum power level but care need to be taken to avoid secondary breakdown problems. However, both devices require sophisticated driving circuitry, snubbing components and complicated short circuit protection schemes for reliable operation. Since increasing switching frequencies is the general tendency in power electronics, this can be increased to reasonably high values by using power MOSFETs. Recently, in many PWM inverters for UPS applications, frequencies above the audio range have been preferred since these inverters require small filtering components and do not generate audible noise [9]. The power MOSFET especially VDMOS appeared to be the most promising device for this and many other applications and it was therefore utilized as the power switching element in the UPS inverter. The structure and the working of the VDMOS is explained in the next chapter.

2.5 UPS Simulation: A NOVEL Approach

The block diagram of the conventional on-line UPS (medium power range) is shown in the figure 2.7.

The input transformer steps down the supply voltage to the required level. The phase-controlled SCR charges the battery. Inverter converts DC to AC (square wave for older UPSs and PWM for recent UPSs). The frequency of the PWM is usually few kHz. This PWM is again stepped up to the required level by an output

transformer. This PWM is filtered by a filter to get the required sine wave. The inverter section consists of the base driver circuit and a power output bridge circuit employing BJTs. The inclusion of input and output power transformers and the use of audio range PWM makes this UPS bulky. Since PWM is not of high frequency therefore filter size is increased considerably. Analog feedback is usually employed this gives rise to the problem of drift caused by component aging.

The block diagram of an on-line UPS using a novel approach is shown in the figure 2.8 . The main difference between this approach and the conventional method are:

- The elimination of input and output transformers.
- Use of ultrasonic carrier frequency for PWM.
- Replacement of primary analog circuit by microcontroller.
- The use of high voltage batteries.
- The use of VDMOS in the inverter section.

The following section will discuss the advantages of the proposed design.

2.5.1 Advantages of The Proposed Design

The advantages of our proposed circuit are:

- The size and weight will be considerably reduced because of the elimination of the input and output transformers.

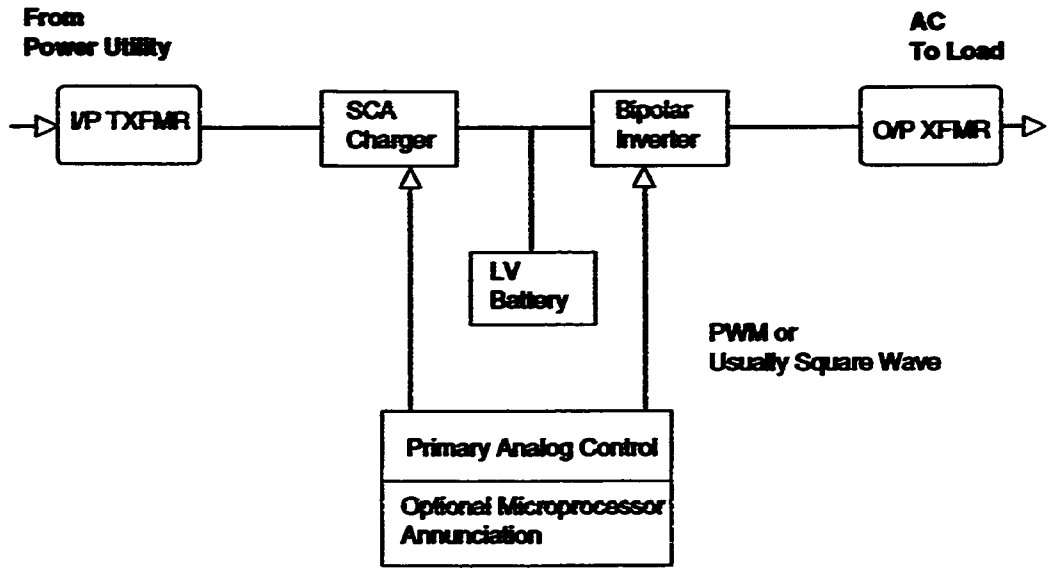


Figure 2.7: On-line UPS

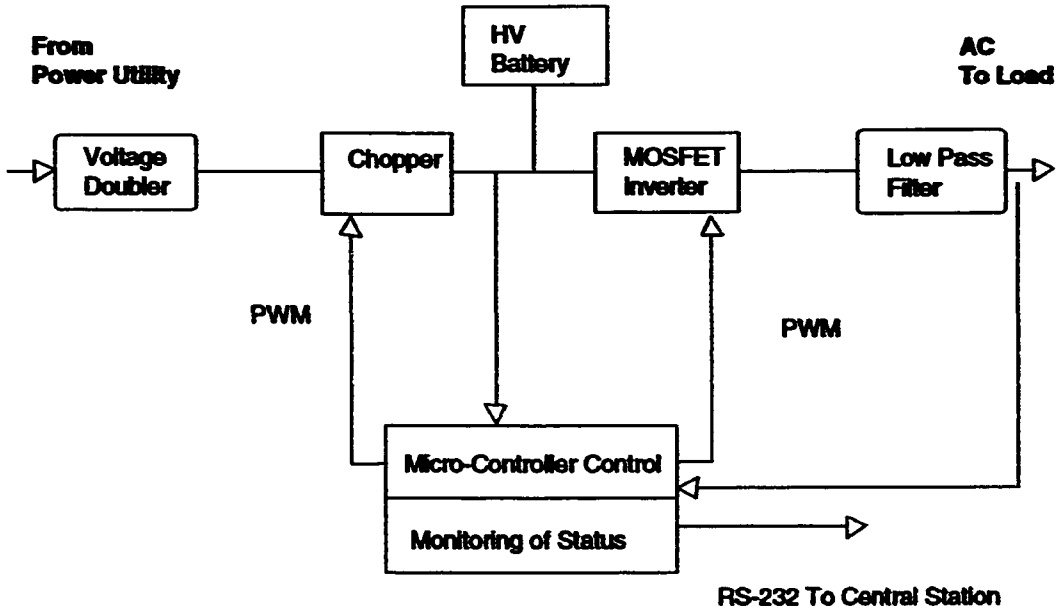


Figure 2.8: Proposed circuit

- Switching speeds above 20 kHz will make a noiseless inverter, whereas in the conventional design the use of BJT does not allow such high speeds to be achieved.
- The size of the filter elements i.e L and C will be reduced considerably.
- The use of high speed microcontroller will allow better control of the output.
- In large industrial organization with many UPSs at different locations, the information related to the status of the systems can be conveyed to a central station where it can be displayed and stored.

2.6 Conclusions

It has been shown that the on-line UPS systems are the only power supplies which provide real protection from all kinds of disruptions in the mains supply. It has also been shown that PWM inverters offer more flexibility in design whilst maintaining the characteristic of being the light weight, and that the VDMOS are the most promising semiconductor devices suitable for ultrasonic PWM inverters in UPS applications.

The next chapter will present the comparison of various PWM strategies available in the literature. The importance of carrier signal in PWM will be emphasized. The methods to calculate look-up table data will be described.

Chapter 3

PWM STRATEGIES AND CALCULATING LUT DATA

The basic principles, advantages and disadvantages of some PWM strategies capable of being utilized in UPS applications are described. The effects of *high frequency carrier signals on the quality of the output waveform* under different operating conditions are discussed together with the importance of carrier signal of 20 kHz. The *regular- sampled symmetric strategy* is discussed in detail. The different methods of calculating the *Look-Up-Table* (LUT) are described together with their advantages and disadvantages.

3.1 PWM Strategies

The aim of such strategies are to *minimize as much low order harmonics* as possible and also to effect control over voltage and frequency with a single switching stage. Several established PWM strategies are available in the literature and these could

be categorized mainly into four types, namely, natural sampling strategy, delta modulation strategy, optimal switching strategy and regular sampling switching strategy.

3.1.1 Natural Sampling Strategy

The natural sampling strategy is based on the *direct comparison of sinusoidal modulating waveform with a triangular carrier waveform* to determine the switching angles and therefore resultant pulse widths are as shown in the figure 3.1. The resultant pulse width is proportional to the amplitude of the modulating waveform at the instant that comparison occurs. Consequently, it is not possible to define pulse widths using analytic expressions. However, it has been shown that as a result of the natural sampling process, which is non-linear, the pulse-widths T_P as shown in figure 3.1 may be defined by a transcendental equation 3.1 [10] .

$$T_p = \frac{T}{2}\left[1 + \frac{M}{2}(SIN\omega_m t_1 + SIN\omega_m t_2)\right] \tag{3.1}$$

- T = Period of the carrier signal
- M = Modulation index = A_c/A_r
- $\omega_m = 2\pi F_m$ = Angular frequency of the modulated signal
- t_1, t_2 = Time instants of sampling of the modulating waveform.

It is not possible to calculate the widths of the modulated pulses directly due to the existing transcendental relationship and this can only be defined in terms of a series of Bessel functions by numerical techniques [10]. This can create difficulties

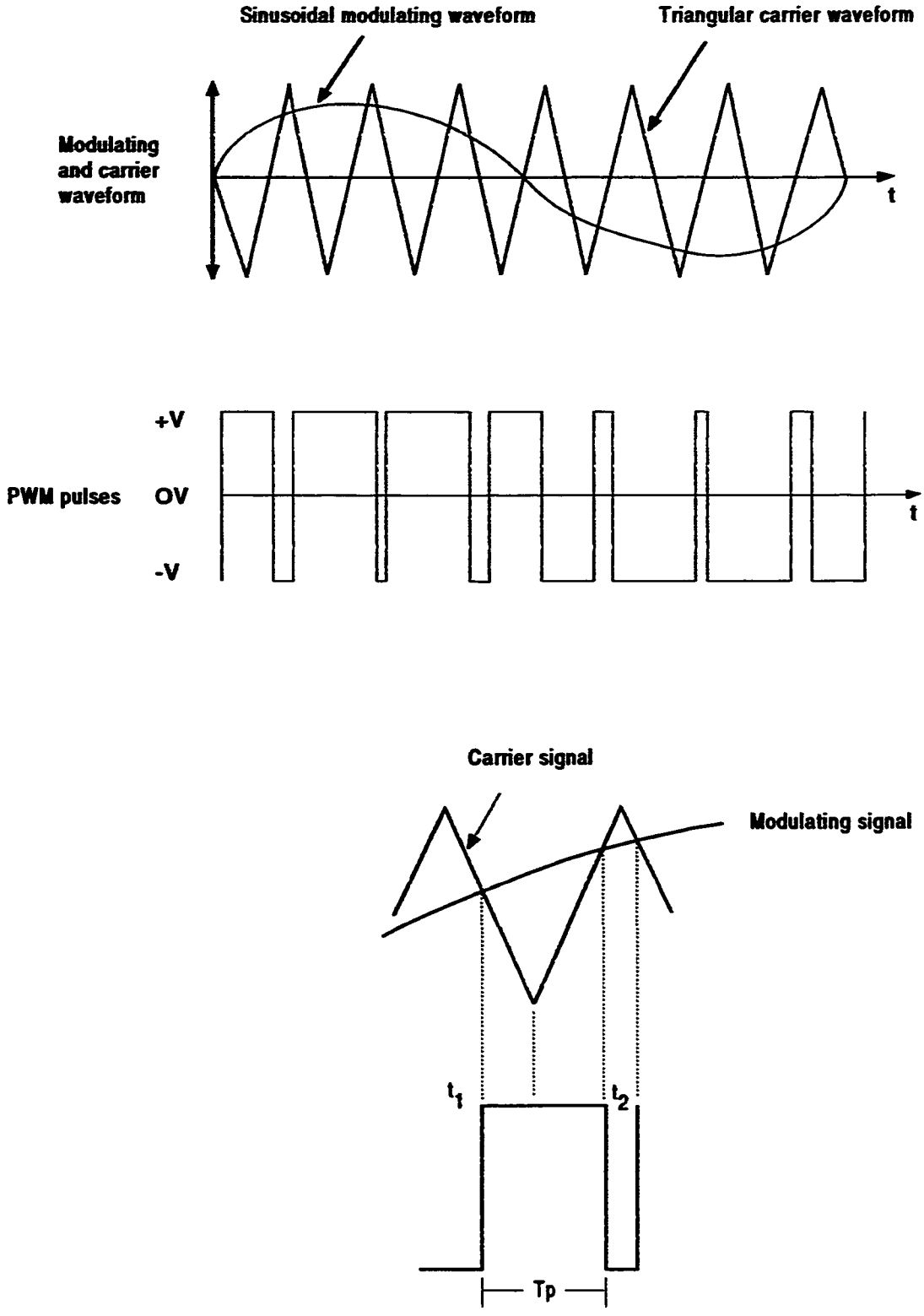


Figure 3.1: Natural sampled PWM process

in computer-aided design analysis and can also make it inappropriate for efficient discrete digital hardware or microprocessor software implementation.

It should be noted that as the carrier frequency is increased, the harmonic content will be reduced because more pulses per cycle in the output wave are obtained. This technique is only widely used in the analogue domain because of its simplicity and ease of implementation using analogue techniques.

3.1.2 Time Optimal Switching Strategies

This method shown in figure 3.2, utilizes a *sine reference waveform Vr and a delta shaped carrier waveform Vc*. The latter is allowed to oscillate within a defined window which has limits equally above and below the same reference waveform Vr. The maximum carrier frequency $f_c max$ can be determined from the minimum window width and the maximum carrier slope. The technique provides inherent constant volts/Hz control for a preset frequency range, a smooth transition of PWM to square-wave mode of operation and it also provides severe attenuation of low order harmonics. This method ensures that a minimum number of components are used when it is implemented using analogue techniques. The principle of PWM generations is shown in figure 3.2.

3.1.3 Optimal Switching Strategies

Harmonic elimination and optimized switching strategies are used to maximize a specified performance criteria such as minimisation or elimination of particular voltage harmonics or minimisation of current harmonic distortion etc. It is recognized

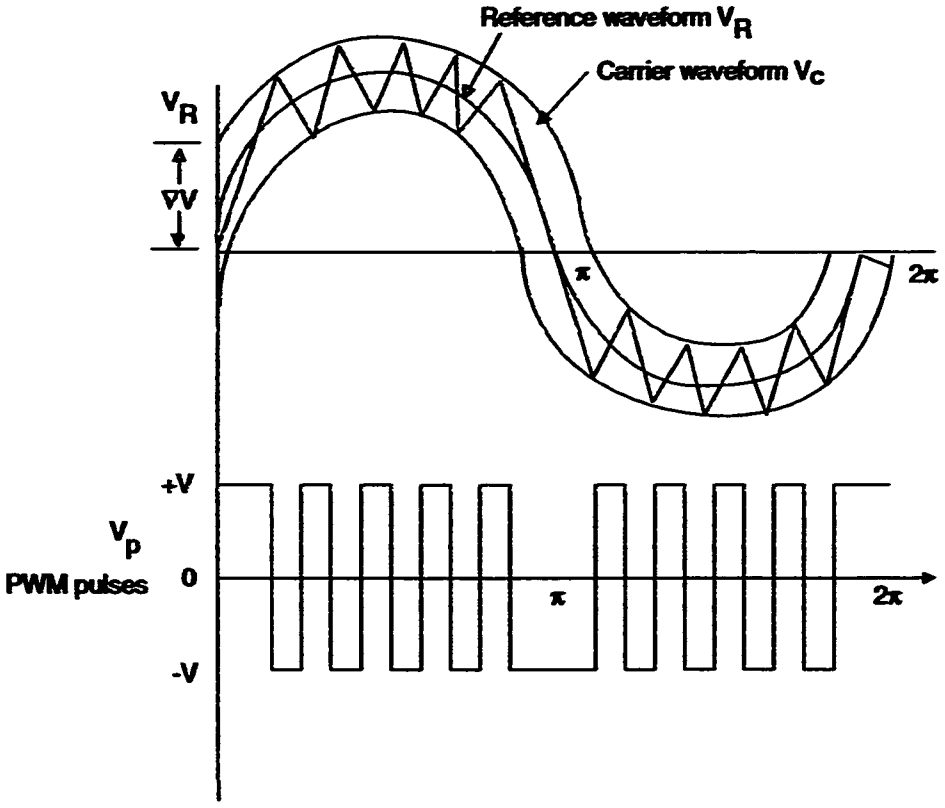


Figure 3.2: Delta modulation waveforms

that these switching strategies can offer significant advantages, even at low frequency ratios, therefore the total harmonic voltage /current distortion can be minimized with minimum switching losses.

These optimized switching strategies *do not rely upon a well defined and recognizable modulation process* of the kind associated with the natural sampled and the regular sampled strategies [11]. All optimized PWM strategies are essentially developed off line using a computer and numerical minimisation techniques to determine the optimized switching angles. Such optimized PWM switching angles are subsequently stored in the microprocessor's memory and used on line to generate PWM pulses in real-time. Thus, there is considerable time, effort and computing resources involved in the development of these optimized switching strategies and also its implementation often requires good switching angle resolution to achieve the predicted performance criteria. These complexities have prevented the use of the optimal strategies in many PWM inverter applications [11].

3.1.4 Regular-Sampled Switching Strategies

The regular sampled PWM strategy is based on a *comparison of the regularly-sampled sinusoidal modulating waveform with the triangular carrier waveform.* It is a well defined modulation process and was proposed by [10]. He demonstrated that this sampling process unlike natural sampled PWM, enables exact defining of the pulses and hence gives a considerable advantage in harmonic cancellation. Furthermore, requlat sampled PWM improves the frequency spectra by reducing the lower frequency harmonics and supressing the harmonics at non-integer frequency

ratios. The regular-sampled PWM strategies are inherently digital, and therefore can be very efficiently implemented using either discrete digital hardware, LSI or microprocessor software techniques.

The regular sampling basically entails the sampling of the modulating wave prior to the comparison with the carrier wave as shown in the figure 3.3. However, the rate at which the modulating wave is sampled depends upon firstly the carrier frequency and secondly upon the type of modulation process. This could be categorized into two, namely, asymmetric and symmetric modulation processes. The regular-sampled strategies can thereby be split up into two, namely, regular-sampled *asymmetric PWM strategy* and *regular-sampled symmetric PWM strategy.*

Regular-Sampled Asymmetric PWM Strategies

In this scheme a sinusoidal modulating waveform is sampled at both positive and negative peaks of the triangular carrier waveform to generate *"sample and hold"* equivalent of the modulating waveform for comparison with the carrier waveform. As a result of the comparison held between these waves, the resultant PWM pulses are determined as shown in figure 3.4. The width of the resultant asymmetrically modulated pulse may be defined in terms of these sampling times as shown in figure 3.4 and can be calculated by equation 3.2.

$$T_p = \frac{T}{2}\left[1 + \frac{M}{2}(SIN\omega_m t_1 + SIN\omega_m t_3)\right] \tag{3.2}$$

It is to be noted that the modulating waveform is sampled at twice the carrier frequency. The method therefore provides more precise but symmetrical modulated

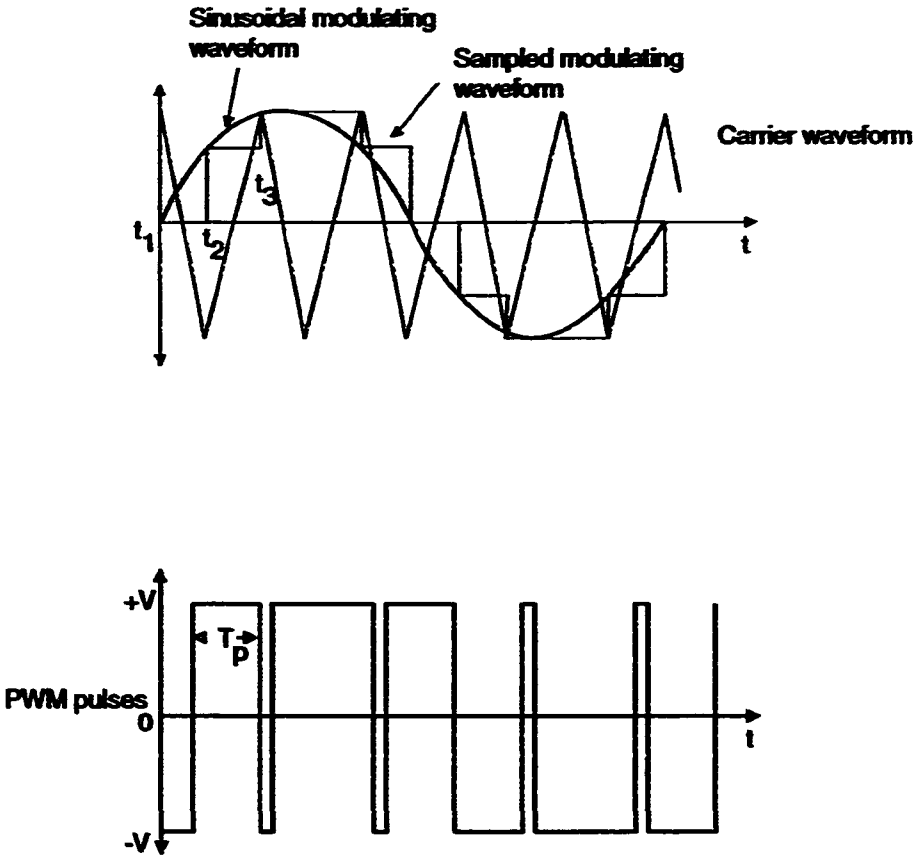


Figure 3.3: Regular sampled PWM

pulses. Its harmonic spectrum is superior to that produced using symmetric modulation. However, it significantly extends the time required for computation when it is implemented by a microprocessor.

Regular-Sampled Symmetric PWM Strategies

This is the simple PWM strategy. In this strategy, the sinusoidal modulating waveform is sampled at every positive peak of the triangular carrier waveform prior to the comparison to be made with the carrier waveform as shown in figure 3.4.

It can be seen from figure 3.4 that the width of each resultant pulse is determined by a single

sample-and- hold value of the modulating waveform, leading to the conclusion that both edges of the resultant pulse are equidistant from their center points.

With reference to figure 3.4 the width of the resultant pulse for symmetric double-edge and single-edge modulation can be expressed as [12, 13].

$$T_p = \frac{T}{2}[1 + MSIN(\omega_m t_1)] \tag{3.3}$$

where T is the time period of the carrier signal.

In contrast to the asymmetric regular-sampled technique, the symmetric regular-sampled technique requires the sampling frequency equal to the frequency of the carrier signal. Thus, it has the *advantage of requiring less processing time over the preceding PWM strategy* when it is implemented by a microprocessor using software techniques.

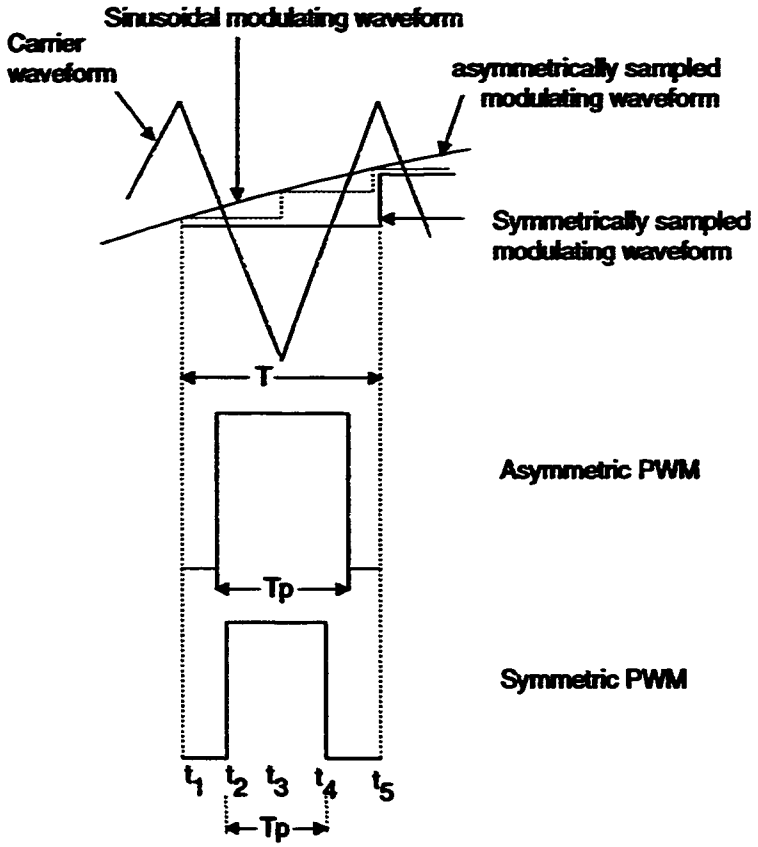


Figure 3.4: Regular sampled symmetric and asymmetric PWM

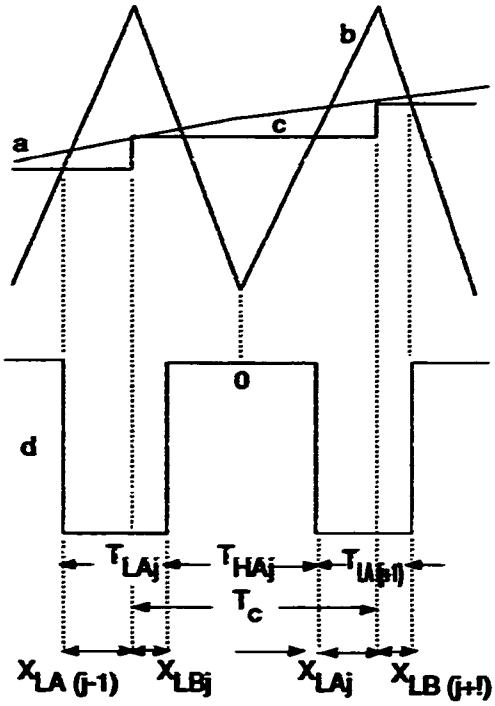
3.2 The Importance Of Carrier Signal In PWM Strategies

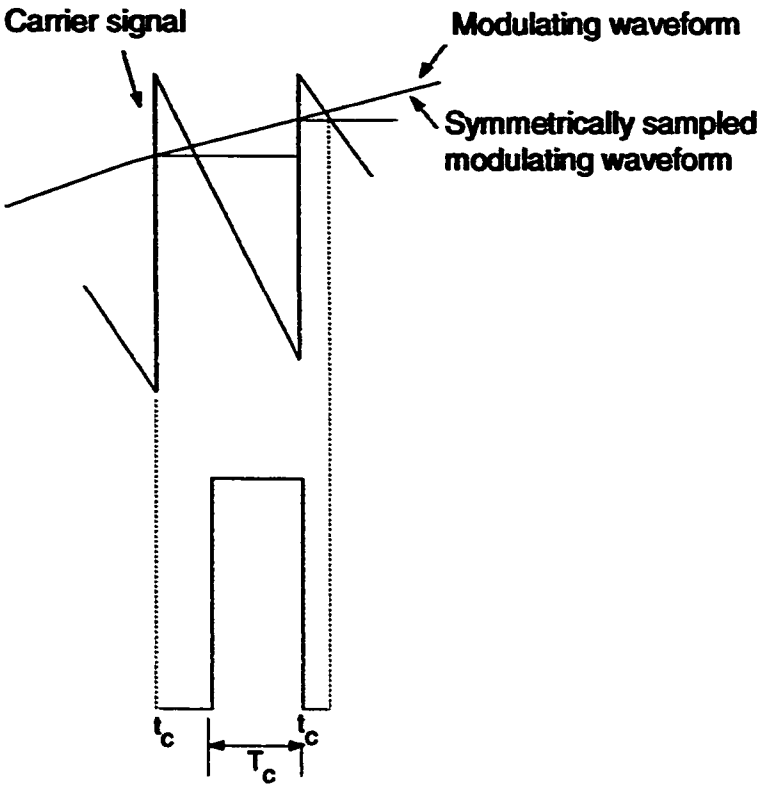
In most of the PWM strategies, the switching angles are determined in relation to the carrier signal. Thus, the shape, the ratio of the carrier signal to the modulating signal and its time-phase relationship with the modulation waveform have certain important consequences on the quality of the output waveform. The following sections illustrate the *effects of a carrier signal on the output waveform* for various categories of PWM techniques.

3.2.1 Single-Edge And Double-Edge PWM

The natural-sampled and regular-sampled PWM strategies can be implemented either using single-edge or double-edge modulation. As shown in figure 3.5 double-edge modulation results by the comparison made between the sinusoidal modulating waveform, whereas the single-edge modulation process uses a saw-tooth waveform as the carrier signal for comparison with the sinusoidal modulating waveform as can be seen from figure 3.5.

Thus, for single-edge modulation, the change in modulation index M results only in one-edge being modulated, the other edge of the PWM pulse remaining fixed (unmodulated), contrary to the double-edge modulation process. Although single-edge modulation results in a waveform with a greater subharmonic content than a double-edge modulated waveform, at high frequencies the amplitude of the subharmonics in both types would be significantly reduced and may be considered negligible. Single-edge modulation has the advantage of requiring less components


a
b
c
0
d
T_{LAj}
T_{HAj}
$T_{LB(j+1)}$
T_c
$X_{LA\,(j-1)}$
X_{LBj}
X_{LAj}
$X_{LB\,(j+1)}$


Carrier signal
Modulating waveform
Symmetrically sampled modulating waveform
t_c
t_c
T_c

as compared to the double-edge modulation [9].

3.2.2 Asynchronous and Synchronous PWM

In general the PWM waveforms are generated as a result of the comparison made between a modulated wave and a carrier wave. If the carrier signal is not synchronized in time phase with the modulating waveform, the PWM generation process is said to be asynchronous. In the synchronous PWM strategy, the carrier frequency is always an integer multiple of the modulating frequency. It has been shown [14] that the synchronous PWM method is much superior to asynchronous PWM scheme with regard to Total Harmonic Distortion(THD). The only criticism about the synchronous operation is that since the carrier and the modulating waveforms have to be synchronized,the carrier frequency must vary over as wide a range as the output frequency. This scheme could advantageously be used in inverters for UPS applications where output frequency is essentially constant [14].

3.2.3 Ultrasonic Carrier Signal

All PWM schemes use a carrier signal at a frequency several times higher than the modulating frequency. From the preceding PWM strategies, it is clear that the *harmonic content in the PWM waveform can be improved significantly* if a higher frequency ratio of the carrier signal to the modulating signal is used. As the ratio of the carrier to modulating frequency is increased, the side bands of the carrier frequency will also move away from the fundamental component. Advances in power Silicon technology allow the switching frequency of the inverter to be increased up to several tens of kHz. The use of carrier frequencies above the audio range have

some important consequences which may be summarized as follows:

1. At higher switching frequencies, the significantly improved harmonic spectra of the output waveform makes it practical to apply the simplest regular-sampled symmetric strategy, either implementing with single edge or double edge modulation [9].

2. A high ratio of the carrier to the modulating frequency provides the wide separation of the fundamental frequency component and the least desirable frequency components in the output waveform. Thus, output filtering can be accomplished with relatively small and inexpensive components.

3. By using ultrasonic carrier frequencies, inverters can be realized without the acoustic noise associated with the magnetic components.

4. Raising the ratio of the modulating frequency gives more precise control over the output waveform synthesisation. By choosing a suitable method of generating the PWM pulses, efficient feedback techniques could be implemented giving control on sub cycle basis.

5. High switching frequencies could decrease the inverter efficiency because of the switching and snubbing losses. These losses can be minimized by incorporating fast switching devices such as power VDMOS which can be operated without the snubbing networks.

6. One difficulty which can arise due to the use of a high carrier frequency for a microprocessor controlled PWM generator, is that the time available to the microprocessor for pulse width computation is very short. In our system using

a carrier frequency of 20 kHz, the width of the pulse has to be calculated within 50 microsecond. A very fast microprocessor with an efficient instruction set is therefore needed, since it is required that it implements all other functions in software required by such inverter.

3.3 The Chosen PWM Strategy

The regular sampled symmetric PWM strategy has been adopted for use in generating the PWM pulses as shown in figure 3.4. Since the modulating and carrier waveforms are synchronized, the first sampling instant t_1 will be equal to Tc/4. The first high level pulse width can therefore can be expressed by equation 3.4:

$$T_{HA1} = \frac{T_c}{2}\left[1 + MSIN\omega_M\left(\frac{T_c}{4}\right)\right] \tag{3.4}$$

Because in the symmetric PWM strategy the modulating signal is sampled once in each carrier period, the second sampling instant t_2 will be held at time instant $(T_c + \frac{T_c}{4})$. The second high level pulse width is then given by:

$$T_{HA2} = \frac{T_c}{2}\left[1 + MSIN\omega_M\left(\frac{T_c}{4}\right)\right] \tag{3.5}$$

and the jth level pulse T_{HAj} is given by

$$T_{HAj} = \frac{T_c}{2}\left[1 + MSIN\omega_M\left(\frac{T_c}{4}\right)\right] \tag{3.6}$$

For achieving double edge modulation, the corresponding low level pulse is given by equation 3.7

$$T_{LAj} = T_c - \left[\frac{T_{HA(j-1)} + T_{HAj}}{2}\right] \tag{3.7}$$

The equation 3.7 involves an addition, a division and a subtraction to obtain the low level pulse widths. The calculation of T_{LAj} can be simplified as follows; since both edges of the PWM pulses are determined by a single sample, both edges are equally modulated or displaced with respect to center points as shown in the figure 3.5. One carrier period can be expressed as :

$$T_c = X_{LAj} + T_{HAj} + X_{LBj} \tag{3.8}$$

and

$$T_c - T_{HAj} = X_{LAj} + X_{LBj} \tag{3.9}$$

X_{LBj} and X_{LAj} are low level pulses before and after the high level pulse width T_{HAj} corresponding to a carrier period. It can be clearly seen from equation 3.9 that the widths of the low level pulses X_{LAj} and X_{LBj} depends on the high level pulse width and the carrier period. Since the widths of both these pulses are equal in value by virtue of the symmetric strategy and the carrier period is constant, the widths of the low level pulses X_{LAj} and X_{LBj} in relation to the prospective carrier period and high level pulse width, T_{HAj} can be calculated from the equation 3.10 [9].

$$X_{LAj} = X_{LBj} = \frac{T_c - T_{HAj}}{2} \tag{3.10}$$

The equation 3.10 may be solved in software by the microprocessor. One mathematical operation in generating T_{LAJ} is eliminated because the high and low level pulses are produced in relation to the prospective carrier period. The complete low

level pulse T_{LAj} between the two consecutive high level pulses, $T_{HA(j-1)}$ and T_{HAj} automatically constructed from

$$T_{LAj} = X_{LA(j-1)} + X_{LBj} \tag{3.11}$$

To achieve single-edge modulation a sawtooth carrier signal is used for the comparison with the symmetrically sampled sinusoidal modulating waveform. With reference to figure 3.5 a low level pulse width T_{LAj} can be calculated directly from the difference between the carrier period and the high level pulse width [9]:

$$T_{LAj} = T_c - T_{HAj} \tag{3.12}$$

Since counters are to be employed to generate the required pulse widths and are decremented at each period of the counter's clock, the actual integer number, ITN_j corresponding to particular pulse width, and which is to be loaded into the counter, is obtained by multiplying the high level pulse width, T_{HAj} by the counter's clocking frequency, f_{ck}. Integer numbers are therefore obtained by solving the equation 3.13.

$$ITN_j = f_{ck}.T_{HAj} \tag{3.13}$$

In a similar manner, integer numbers corresponding to the low level pulses X_{LBj}, X_{LAj} and T_{LAj} can be obtained to implement double-edge and single-edge modulation. The corresponding equations may be written as

$$ITN_{Dj} = f_{ck}.X_{LAj} \tag{3.14}$$

for double edge modulation and

$$ITN_{sj} = f_{ck}.T_{LAj} \tag{3.15}$$

is for single end modulation.

As can be seen from the above equations, the calculation of the integer numbers corresponding to the pulse widths T_{HAj} involves additions, multiplications and sine function. Thus if above equations are to be solved on line, considerable time consuming computations would be required to obtain the integer numbers ITN_j. A software based implementation using a general purpose microprocessor is therefore not possible especially when a high carrier frequency is to be utilized. It was therefore decided to calculate the integer numbers off-line, corresponding to the high level pulse widths. To maintain the output voltages at a fixed level under different supply voltages and load conditions, solving for M=0.75 to 0.975 with a step of 0.005 for a quarter of a cycle and the results are stored in the form of Look Up Tables(LUT).

3.4 Methods of Calculating the Look Up Table Data

As explained above, the calculations involved in solving equations 3.4 through 3.15 for regular sampled symmetrical PWM are performed off line, and the results stored as Look Up Tables. This scheme therefore increases the throughput of the general purpose microprocessor which would also be capable of performing more efficiently other functions required by the system. There are two methods of performing the off line calculation of the LUT data during initialization and calculation of LUT data using a separate system.

3.4.1 Calculation Of LUT Data During Initialization

This technique requires the use of additional hardware or software packages with the existing microprocessor to perform the required calculations. The hardware component may consist of an Intel 80287 math coprocessor which can be used as a parallel processor. This numerical processor is expensive and, if used would add to the cost and complexity of the system. For these reasons an alternative method namely, emulation of 80287 by software was considered.

Since an intel 80286 microprocessor is to be used, the trigonometric and arithmetic capabilities of the 80287 may be realized by using the emulation software instead of employing the 80287 itself. This method requires nearly 32k of memory space and takes a *considerably long time* which is deemed unacceptable.

3.4.2 Calculation Of LUT Data On A Separate System

The disadvantage of the previous system can be overcome by calculating the LUT data before hand. Usually, this involves the use of a separate computer for the calculations of LUT data which is then transferred into the memory of the dedicated computer.

3.5 Conclusions

The synchronous regular sampled PWM strategy is chosen since it has the advantage over other PWM schemes of requiring a minimum number of calculations to generate the PWM pulses. The equations derived to calculate the low level pulses require less computation time and enable the system to generate low and high level

pulses corresponding to the prospective carrier period.

The next chapter will deal with the design and simulation of different parts of PWM UPS on SPICE package. A VDMOS model will developed and incorporated into the SPICE package. The inverter section, output filter, and high speed gate driver will be simulated. Battery selection will be discussed. Doubler and battery charger will be simulated.

Chapter 4

DESIGN AND MODELING

This chapter describes the design and simulation of the various building blocks of a PWM UPS. The design and simulation of PWM generation process will be described. Since SPICE doesn't support VDMOS model so a model will be developed. Simulation of VDMOS will be carried out, static as well as dynamic characteristics will be verified. Next section deals with the design of the base driver. Power stage is a bridge type employing VDMOS as power handling components. Various parts of the UPS are simulated using PSPICE.

4.1 PWM Generation Process

As described previously, the integer number corresponding to high level pulse T_{HAj} are calculated for a quarter of a cycle. These integer number may be transferred to the EPROM or ROM as lookup tables. These lookup tables may be used to calculate the pulse width. PWM generation process for an actual circuit, and a simulated circuit is described in the following sections.

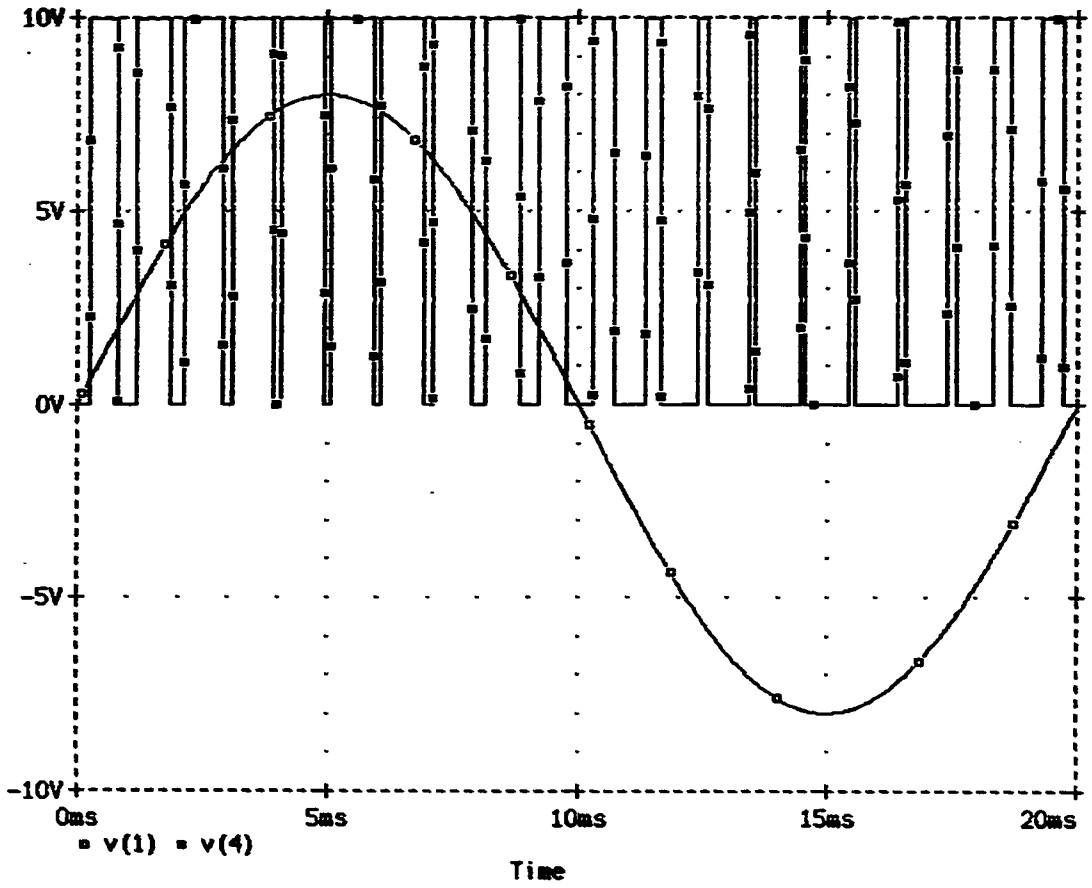
4.1.1 Actual Design

Since integer numbers ITN_j corresponding to the $THAj$ are stored in the EPROM for a quarter of a cycle for different modulation indices, the microprocessor completes calculations for a half cycle and transfers the data into the RAM as the look-up-tables data. A counter is employed to generate the PWM pulse. The counter is loaded with the integer number ITN_j, the output of the counter will remain low while it is counting and will become high at the end of the count. The counter can be loaded with the new value of integer number without disturbing the count in progress. The counter is started after the end of carrier period. Due to the constant period of the carrier frequency, the low level pulse width T_{LAj} is automatically found. This eliminates the need of calculating T_{LAj} by the microprocessor. Thereby this PWM generation process simplifies the design of the single-phase PWM generator.

4.1.2 Simulation of PWM

SPICE is used to simulate the UPS, and it has no provision for the generation of the PWM. Two different methods were devised. First one used analog technique to generate natural sampled PWM, triangular wave and a reference sine wave were compared to produce PWM as shown in figure 4.1. The other was a digital method it used look-up-table to generate regular sampled PWM. Look-up-table method is discussed below.

- The value of T_{HAj} corresponding to high level pulse was stored in the file for quarter of a cycle, for modulation indices varying from .75 to .975 in .005 steps. Since the frequency of the carrier was 20KHz, therefore total enteries were 4600. Program to generate look-up table data is given in appendix B.3.



V(1): Reference sine wave ; V(2): Generated PWM

Figure 4.1: PWM generation process

- The spice *.cir file was run for one pulse, the next pulse width was put into the file, by another program from the lookup table.
- The output voltage at various nodes in *.out file was read and was substituted in the *.cir file as initial conditions, so that the actual working of the circuit is not disturbed.

4.2 VDMOS Model for PSPICE

The ever increasing switching frequency of semiconductor devices in new power processing topologies *needs a good characterization of the power transistor*, namely the accurate evaluation of its internal capacitances. In a low frequency switching power circuit, the effects of the transistor switching times and internal capacitances are negligible. In this case the transistor can be modeled as a resistor in the on state and as an open circuit in the off state and the transitions between those two states can be taken as instantaneous. In a *high frequency switching mode power circuit such as PWM inverter, the switching times and internal capacitances are very important*, because they limit the power efficiency and the maximum frequency of operation of the circuit [15, 16]. A basic but an accurate model for switching circuits with resistive and inductive loads is described. It works well for low as well as high voltage devices. Its configuration is based on the model, whose parameters are related to the physical properties and topology of the VDMOS transistor. The topology of the VDMOS transistor is shown in the figure 4.2. We notice from the schematic that:

- The conduction channel is represented by current generator Jd

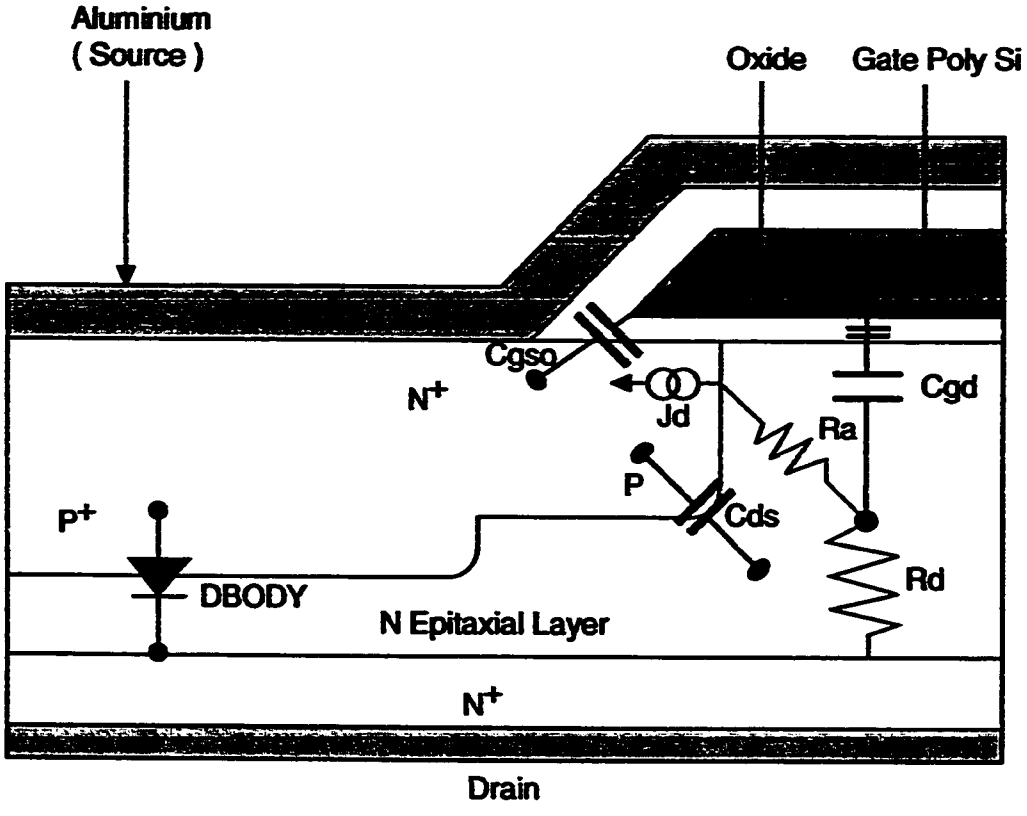


Figure 4.2: Cross section of the VDMOS

- The n-type layer between the p wells with the access resistance Ra to the channel and the highly non linear gate capacitance Cgd.
- The low doped n-type epitaxial bulk accounted for by the drift resistance Rd and the pn junction capacitor Cds.
- The gate metallization overlap of the N+ source diffusion which creates, through the thin and thick oxide, a constant parasitic capacitor Cds.

When the VDMOS transistor goes through a switching phase, all the three different modes: Blocked, Ohmic and Saturation are involved. The model as shown in the figure 4.3 takes into account all three operating modes [17]. This VDMOS Transistor model cannot be described by a single component of the SPICE library. A *macro model has been constructed* in which, each element is part of this model library. The current generator Jd, for example is represented by the MOS model. The Cgs is considered to be constant as a first order approximation. Rd and Rd are constant too. The macro model schematic for an N channel device is shown in the figure 4.4. The SPICE listing of a VDMOS is shown below.

```
.SUBCKT  MTP3055E  20  10  30
RG  10  1  10
M1  2  1  3  3  DMOS  L=1U  W=1U
.MODEL  DMOS  NMOS  (VTO=3.32 KP=5.5  THETA=.058 VMAX=1.4E5 LEVEL=3)
CGS  1  3  300P
RD  20  4  0.089
DDS  3  4  DDS
.MODEL  DDS  D (M=0.42 CJO=608.1P VJ=0.60)
```

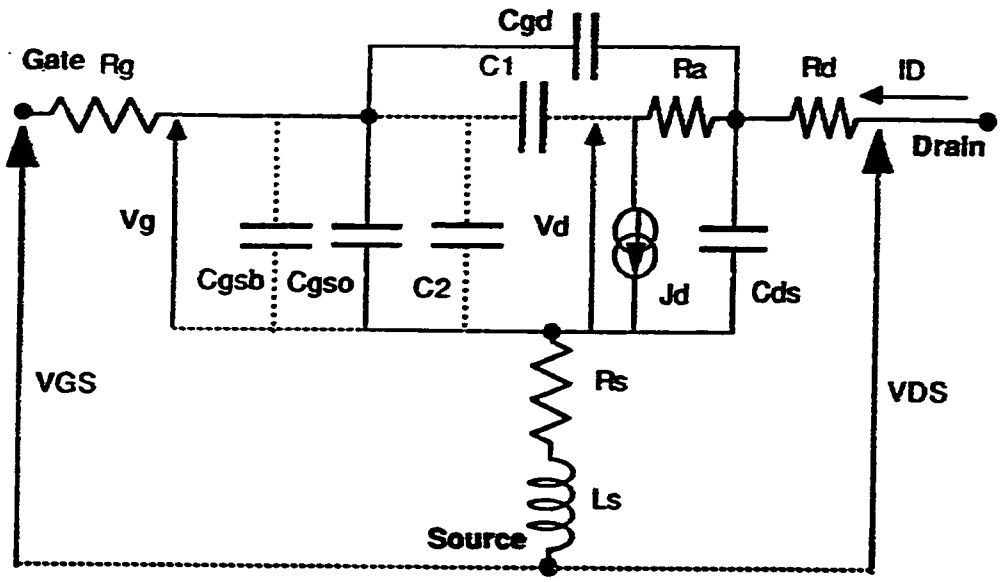


Figure 4.3: Simplified model of the VDMOS power transistor

```
DBODY  3  20  DBODY
.MODEL  DBODY D (BV=60  IS=1.1E-11  N=1.03 RS=0.50 TT=200N)
RA  4  2  1E-3
RS  3  5  1M
LS  5  30 5N
M2  1  8  6  6  INTER
E2  8  6  4  1  2
.MODEL INTER NMOS (VTO=0 KP=10 LEVEL=1)
CGDMAX  7  4  605P
RSGD  7  4  1E7
DGD  6  4  DGD
RDGD  4  6  1E7
.MODEL DGD  D (M=0.53 CJO=605P VJ=0.08)
M3  7  9  1  1  INTER
E3  9  1  4  1  -2
.ENDS
```

The subcircuits for two different type of VDMOS are given in appendix A.6 and A.7. The tests carried out to verify the correct working of the VDMOS were.

- The Static Characteristics.
- Dynamic Characteristics.

The achieved model accurately represents the static and the switching performance of VDMOS device. The results of the both the tests are shown in the figures. Figure 4.5 shows the static characteristics of the VDMOS. Figure 4.6 represents

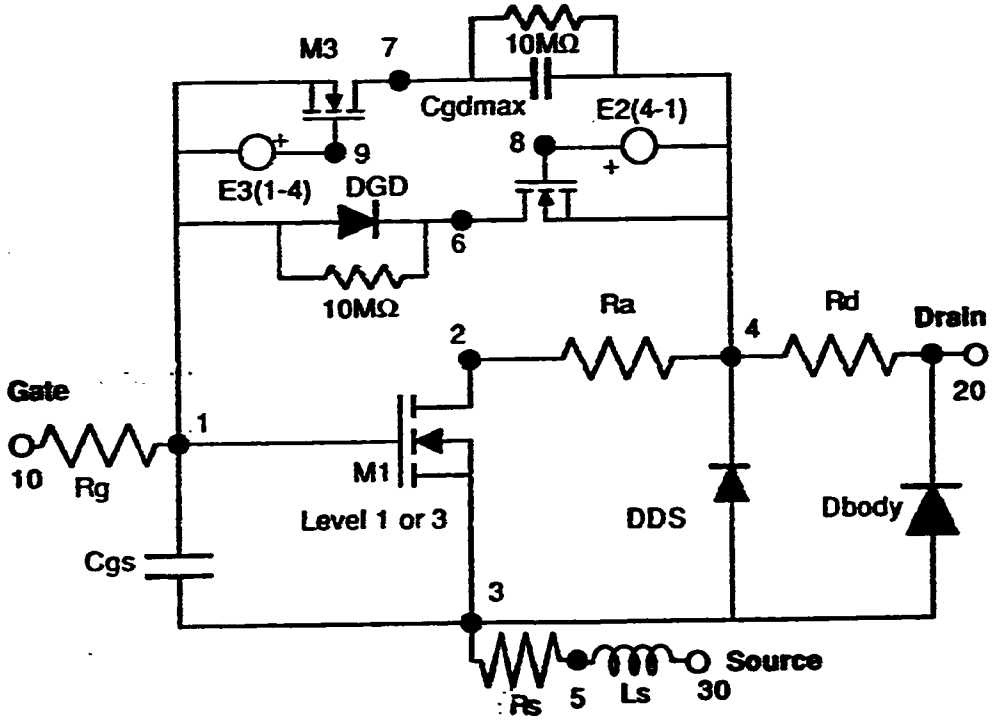


Figure 4.4: Block diagram of the macro model of VDMOS used for simulation

the switching characteristics with resistive load and figure 4.7 depicts the switching characteristics with inductive load. Instantaneous power loss of the device is shown in figure 4.8. The SPICE listing to model the circuits for determining the switching, static and dynamic characteristics of VDMOS are listed in appendix A.8, A.6, A.7 respectively.

4.3 Gate Driver

The gate drive requirements of a power VDMOS are much more simpler than other gate controlled devices discussed in chapter 1. Many papers and application notes have been written about driving power MOSFETS directly from CMOS or open-collector TTL logic. Although these schemes seem to be very attractive in terms of the simplicity, but *driving the gate from these sources may reduce the switching times of the MOSFET and make it too slow for high speed applications.* The reason is that when a MOSFET is driven by such type of a device, the loss of its potentially high speed switching characteristics is actually due to the limited peak out put current available to charge or discharge the effective gate to source capacitance. The large the die area of the power MOSFET being driven the larger is the effective gate to source capacitance. As a result the total gate charge required to change the gate source voltage to the required value may also increase. Logic gates, with their very limited peak output current capability, are inevitably the limiting factors if used as gate drivers for high power MOSFETS [18].

Another phenomenon known as the *"Miller effect"* also takes place and causes the effective gate to source capacitance of a common source connected power MOSFET

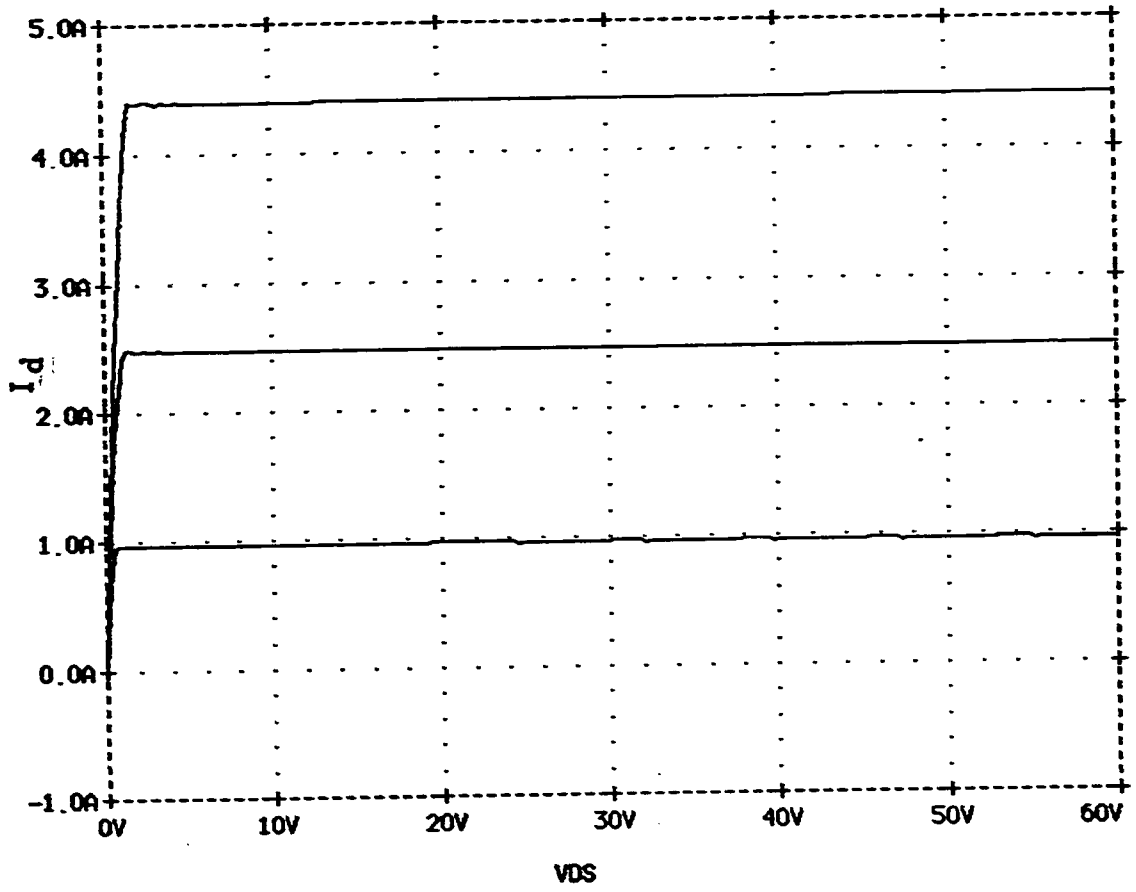


Figure 4.5: Static characteristics of the VDMOS

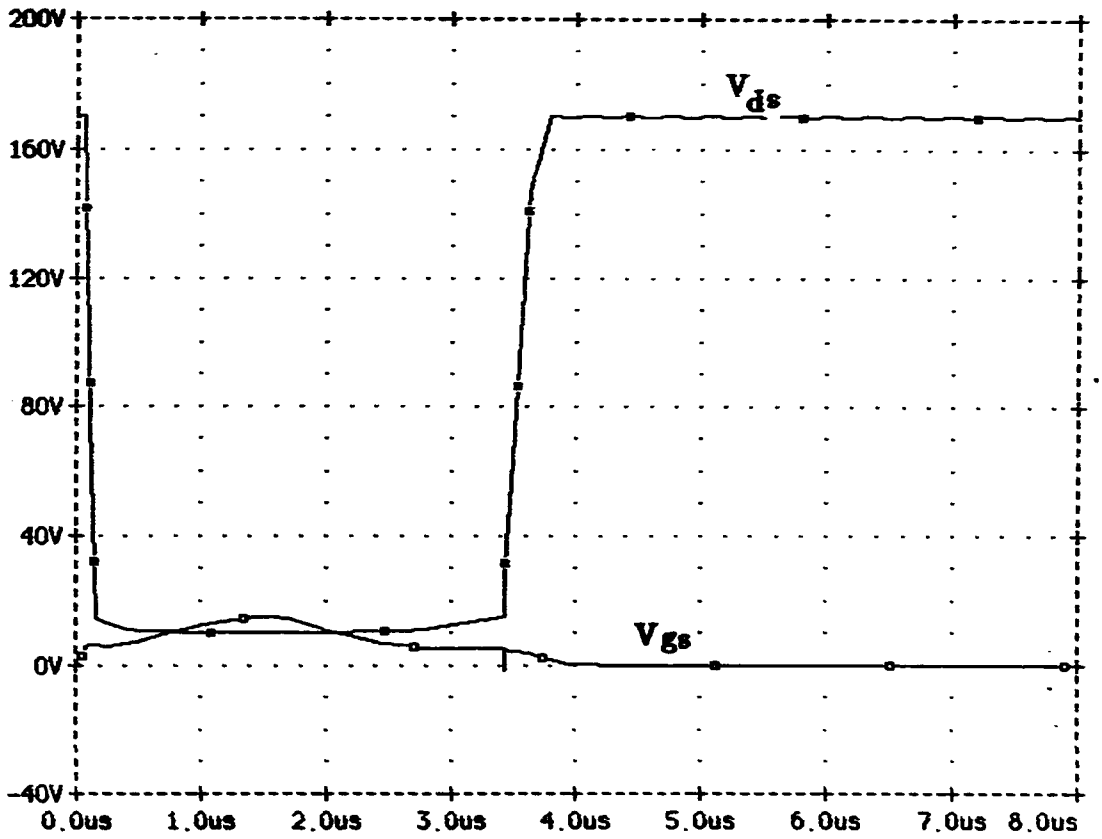


Figure 4.6: Switching characteristics with resistive load

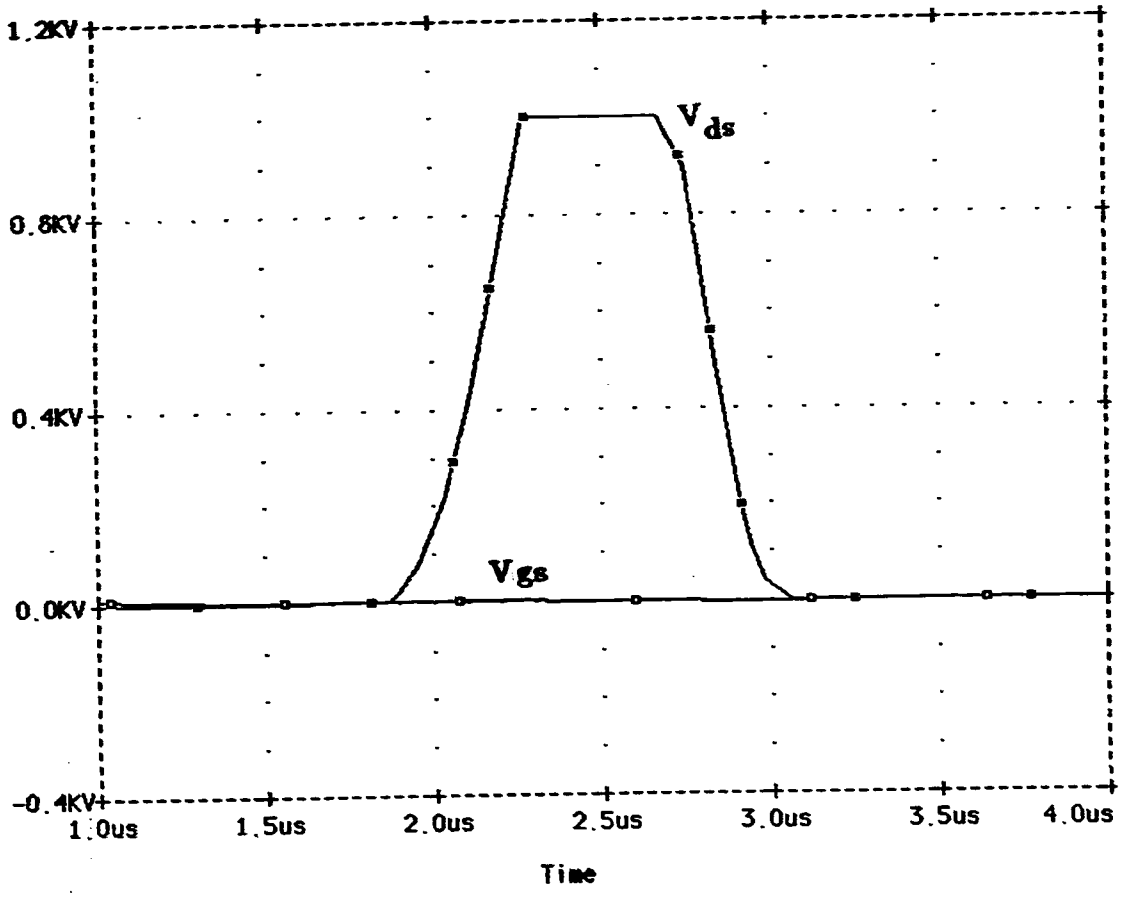


Figure 4.7: Switching characteristics with inductive load

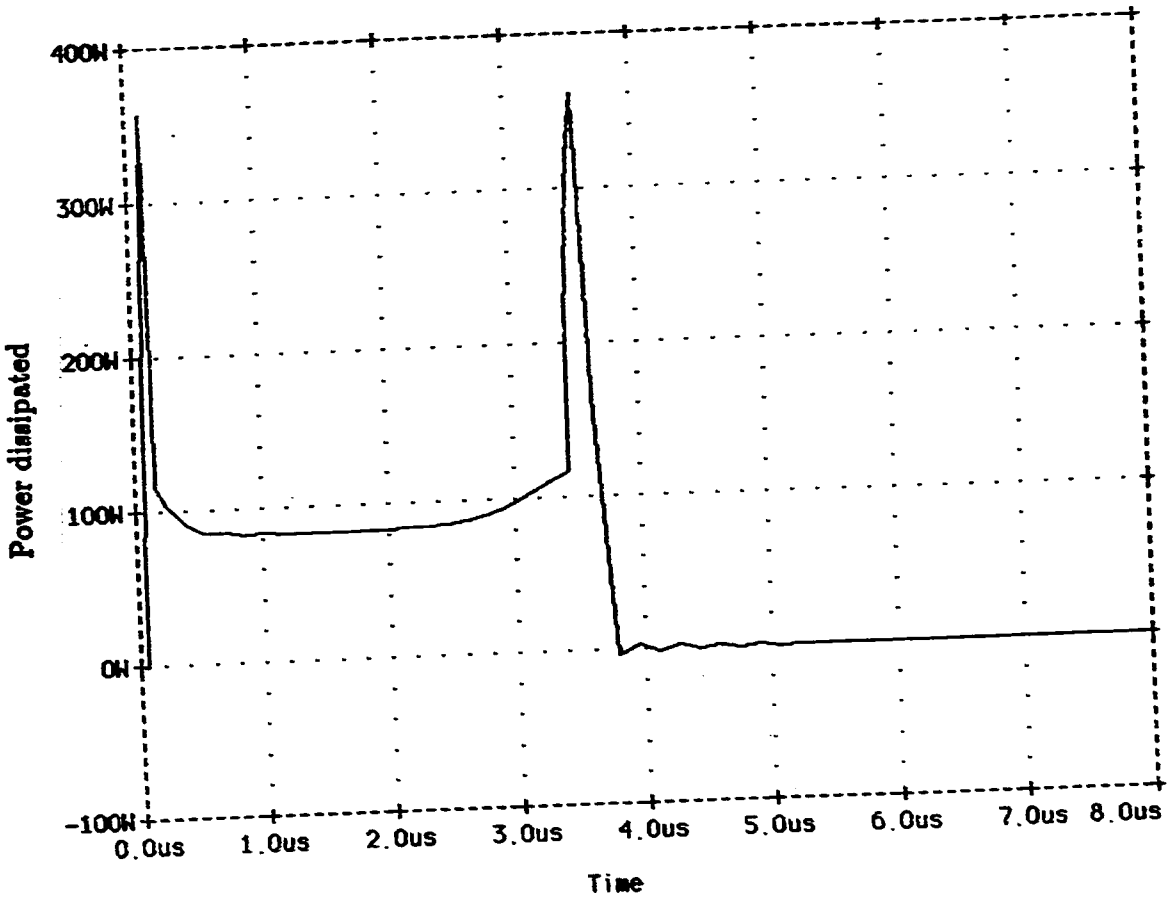


Figure 4.8: Instantaneous power losses

to assume a much larger value than its static specification during a switching transition. In high speed gate drive circuits, it necessitates a substantial peak output current capability. The total drive power needed is small since only the short pulses are required to charge/discharge the gate-source capacitance, and hence simple gate driver circuits can be used.

4.3.1 Need for Isolation

Many switching applications involve driving the power component from control logic or other circuitry that is ground referenced. To drive a power VDMOS whose source is not ground referenced the need for some form of the DC isolation between either the control logic and the driver, or between the driver and the VDMOS is required.

There are basically two standard methods that can be used to provide the DC isolation between the MOSFET and its associated control circuitry are [18].

- Transformer Isolation
- Opto-coupler Isolation

Both type of circuits are shown in the figure 4.9. Next section will discuss the design and the working of both of the circuits.

4.3.2 Design Stage

The gate drive circuit must provide *isolation between the power stage and the control circuitry* and must be capable of handling large duty ratios. As discussed optocoupler and transformers are the best known devices to achieve DC isolation. The opto

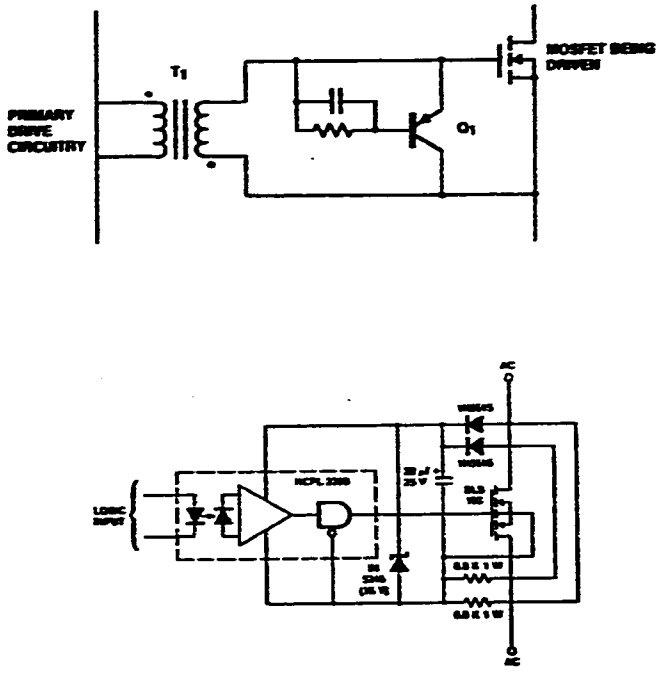


Figure 4.9: Isolation using pulse transformer or opto-isolator

isolator requires extra floating power supplies, whereas the main difficulty normally associated with the latter is that the transformer core flux must be reset every half cycle to avoid saturation. This is rather difficult to achieve with PWM signal since the volt second products are different in each half cycle due to the nature of the PWM pulses.

The PWM wave can be transmitted as a series of short on/off pulses corresponding to the rising and falling edges of the PWM pulses. In this scheme two separate pulse transformers are used to transmit on and off pulses to the MOSFET where on pulse charge the gate capacitance through a diode which becomes reverse biased when the pulse is removed thereby allowing the MOSFET to remain charged due to the charged gate capacitance. The second (off pulse) turns on a bipolar transistor connected in parallel to the gate source capacitance to discharge the capacitor. The MOSFET remains in the off state until an on pulse is applied. The disadvantage of this circuit is that it requires pulse transformers and the design becomes bulky and inefficient.

The circuit proposed for use in the present application uses *opto couplers* to provide the required isolation. The PWM signal is fed through the optocouplers and then connected to the H bridge circuit through the high speed drivers, D469A from Siliconix. The functional block diagram of D469A and the complete circuit of the gate driver for the four legs of the bridge is shown in the figure 4.10. The use of the gate driver and opto isolators, makes an efficient drive circuit which is compact, simple, and has low cost.

4.3.3 Modeling the Gate Driver

After the design of the base driver comes the problem of simulation. D469A is a quad high speed MOS driver, it can source or sink current up to 1.5A . Each driver in the D469A may be configured as being logically inverting or noninverting. The circuit used to model the current source driver D469A from siliconix is shown in the figure 4.12 [19].

4.3.4 Switching Lag Times

It is a common practice to provide sufficient length of lag- time between the switching off of the upper device and the switching on of the lower device in the same leg of an inverter bridge circuit. By doing so the devices will not be able to conduct simultaneously, thus avoiding a direct short circuit, this process introduces low order harmonics in the output waveform. During the lag time, when both switching devices are off, the output potential will be determined by the load current instead of the switching devices. In this period one of the phase diodes will be conducting which effectively connects the load to the positive or negative DC line as shown in figure 4.13. The potential developed during lag-time is a part of the output waveform and is responsible for introducing the unwanted low order harmonics.

Extensive studies have been carried out [20, 21] to establish the degree of the distortion and its dependence on the relationship between the *carrier frequency and lag-times.* It is recommended that the product of the lag time and the carrier frequency should be kept as small as possible to obtain an output waveform with minimized additional distortion. It is clear from the result contained in the above

references that harmonic distortion depends on the magnitude of the lag time employed, whereas the required lag time depends on the type and the size of the power switching devices utilized. When power MOSFETs are to be employed, lag times in the range of a few hundred nano seconds can be used, In our application the lag time has been kept to minimum.

4.4 Power Stage and Filter

The circuit diagram of the complete single phase bridge inverter along with the gate driver is shown in the figure 4.11. For the sake of simplicity and to save simulation time half bridge inverter is simulated. Functionally it is same as full bridge inverter. The only difference being that of a double power supply as shown in the figure 4.13. VDMOS were used as the switching devices in the circuit. Diodes are employed in series with each VDMOS to prevent the body diode from conducting. This stage is driven from the base driver simulated in the preceeding section. Since the ratio of the carrier to the modulating frequency is high therefore simple LC filter can be used [22]. As spice doesn't support the generation of PWM a *macro model for PWM generator was created using the natural sampling approach.* The base drive is driven from a PWM source to drive the VDMOS bridge. The output of the inverter is fed to the LC filter to remove the higher order harmonics. The output of a bridge consisting of a VDMOS, and that of a bridge consisting of an ordinary MOSFET IRF250 is shown in figure 4.14 and figure 4.16 respectively. The instantaneous power dissipation for both the devices is shown in the figure 4.15 and figure 4.17. PSICE listing for modeling the gate driver and the inverter stage along with the filter elements is given in appendix A.3. It is evident that the performance of the

VDMOS is better than that of IRF250. PWM generator base driver and inverter are for the time being connected in open loop configuration i.e without any feed back.

4.5 Doubler and Battery Charger

UPSs usually have a transformer at the input which steps up or steps down the input voltage for the battery charging. In the proposed approach the input transformer has been eliminated. This has been made possible by the following changes in the conventional UPS design.

- replacing the low voltage battery with high voltage battery
- Voltage doubler has been used instead of the bulky transformer.
- The use of high voltage battery eliminates the need for an output transformer.

The complete doubler and battery charger section is shown in the figure 4.18. The output of the doubler is shown in the figure 4.20.

4.5.1 Batteries: PSPICE Model

Batteries for emergency/standby systems are assembled from lead acid or nickel cadmium cells to meet the requirement for voltage, discharge current, duration of discharge and other factors [23]. Batteries may consist of primary cells (nonrechargeable) or secondary (rechargeable) cells. The proposed design uses only the secondary batteries. The use of Nicads is recommended for the UPS, because generally it is

more rugged, requires less maintenance and exhibits a longer life. The charge discharge curves for a nicad battery are shown in the figure 4.19. Battery voltage is maintained constant by utilizing the uniform pulse width control. The use of PWM ensures that the PF can be kept close to unity [24]. In case of the power failure the load is supplied from the battery. The battery is simulated by a high value capacitor in series with a small resistor. The voltages at various points of the battery charger are shown in the figure 4.20. PSPICE listings for modelling the doubler and the chopper section along with the batteries are shown in appendix A.4 and A.5. It is clear that this arrangement works well, thus eliminating the need for an input as well as an output transformer. Making the design efficient and compact.

4.6 Conclusions

In this chapter the design and simulation of the various components of a UPS has been presented. The actual PWM generation method and a novel method to simulate PWM in SPICE is described. VDMOS model has been developed and this model has been substituted as a switching element in the inverter and charger section. The model for high speed gate driver has been developed. The comparison of the output from MOS and VDMOS inverter has been presented.

Next chapter presents the lab implementation of the various building blocks of the UPS. The unique method of digital feedback simulation has been discussed and the results presented. Various monitoring and diagnostics schemes are discussed.

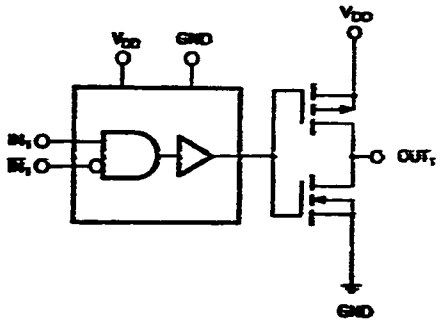


Figure 4.10: Functional block diagram of the D469A

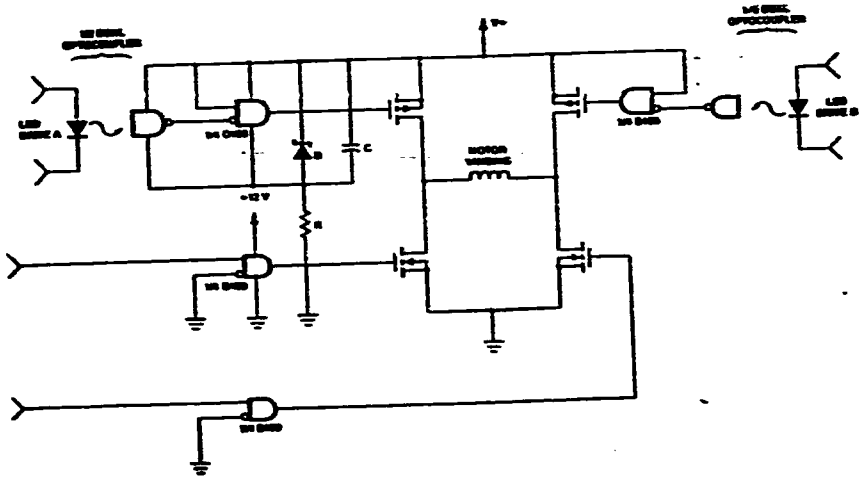


Figure 4.11: Complete circuit of the gate driver and inverter

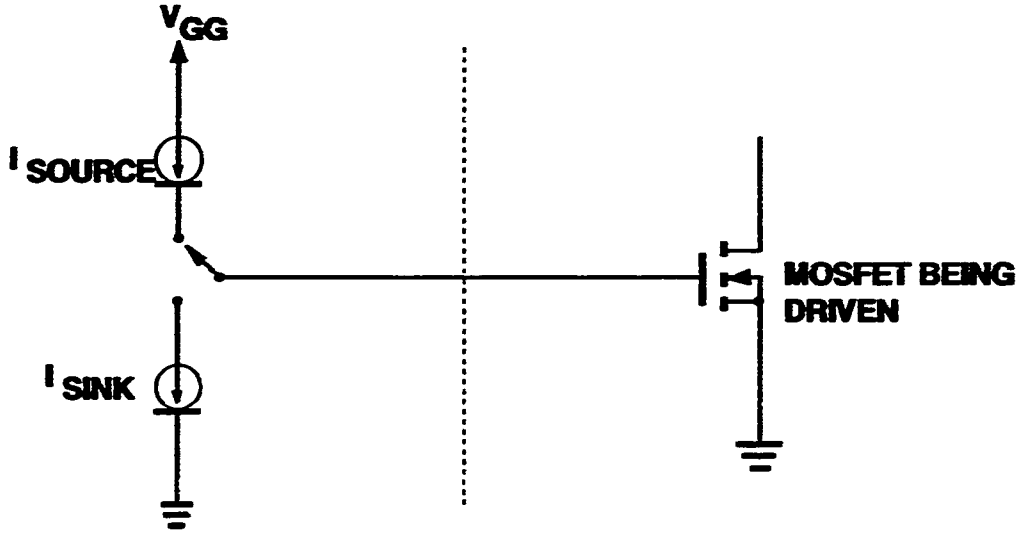


Figure 4.12: Circuit to model gate driver

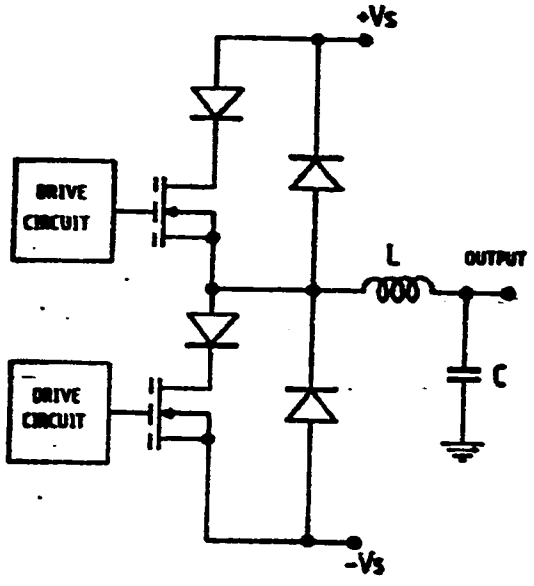


Figure 4.13: Half Bridge

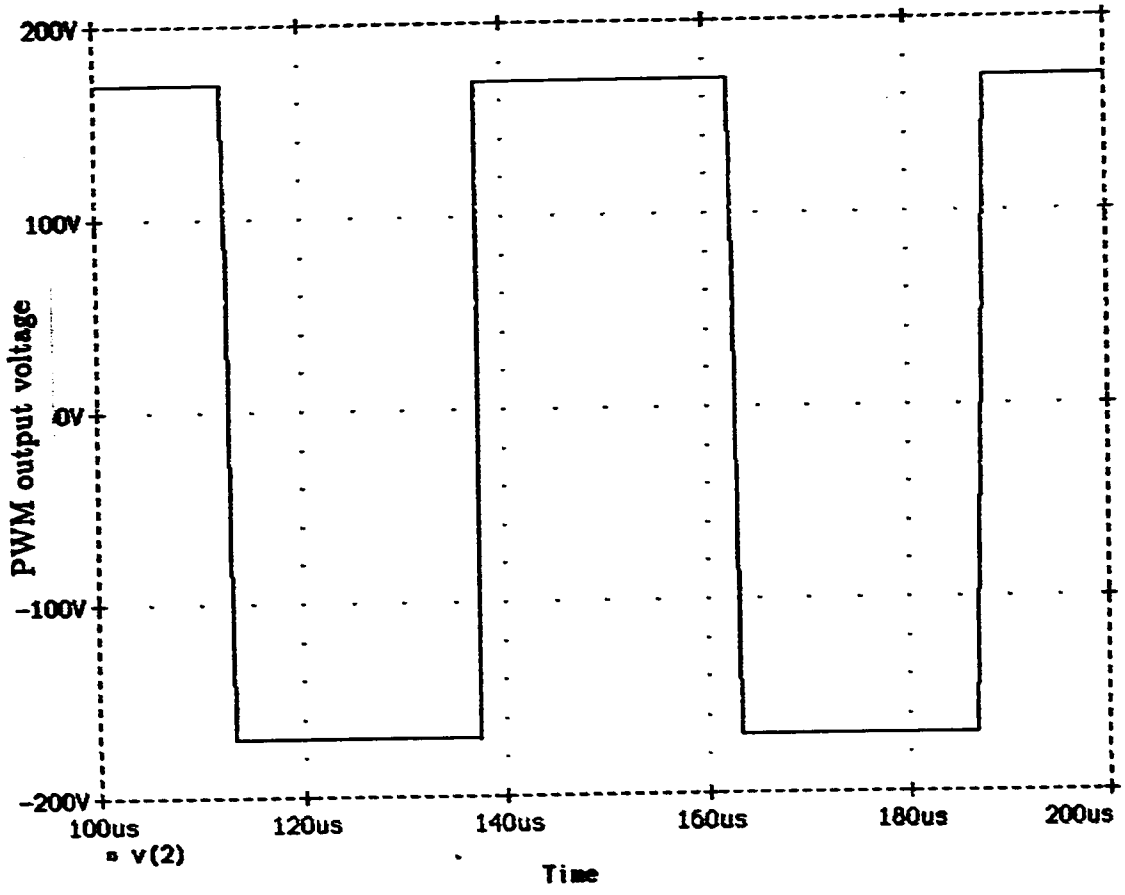


Figure 4.14: Out put PWM filtered out for VDMOS bridge

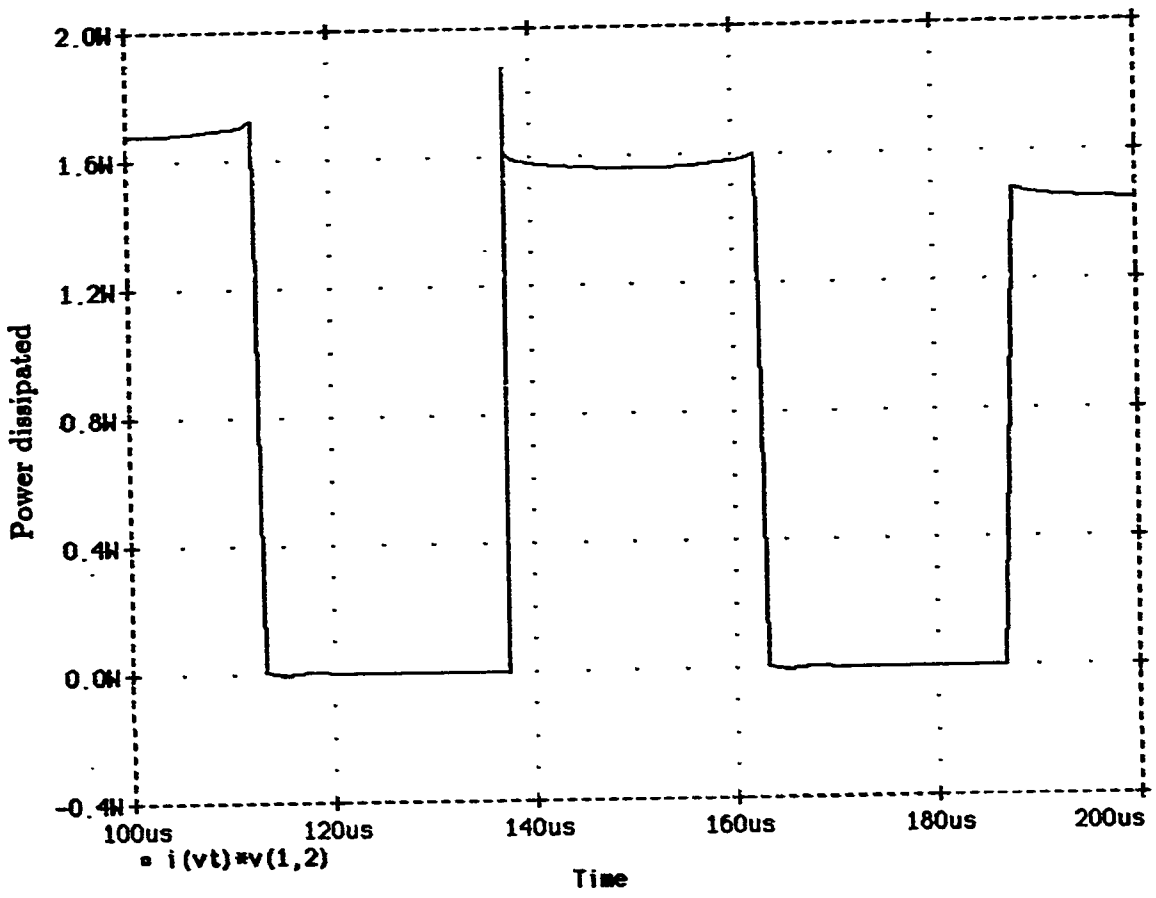


Figure 4.15: Instantaneous power dissipation for VDMOS bridge

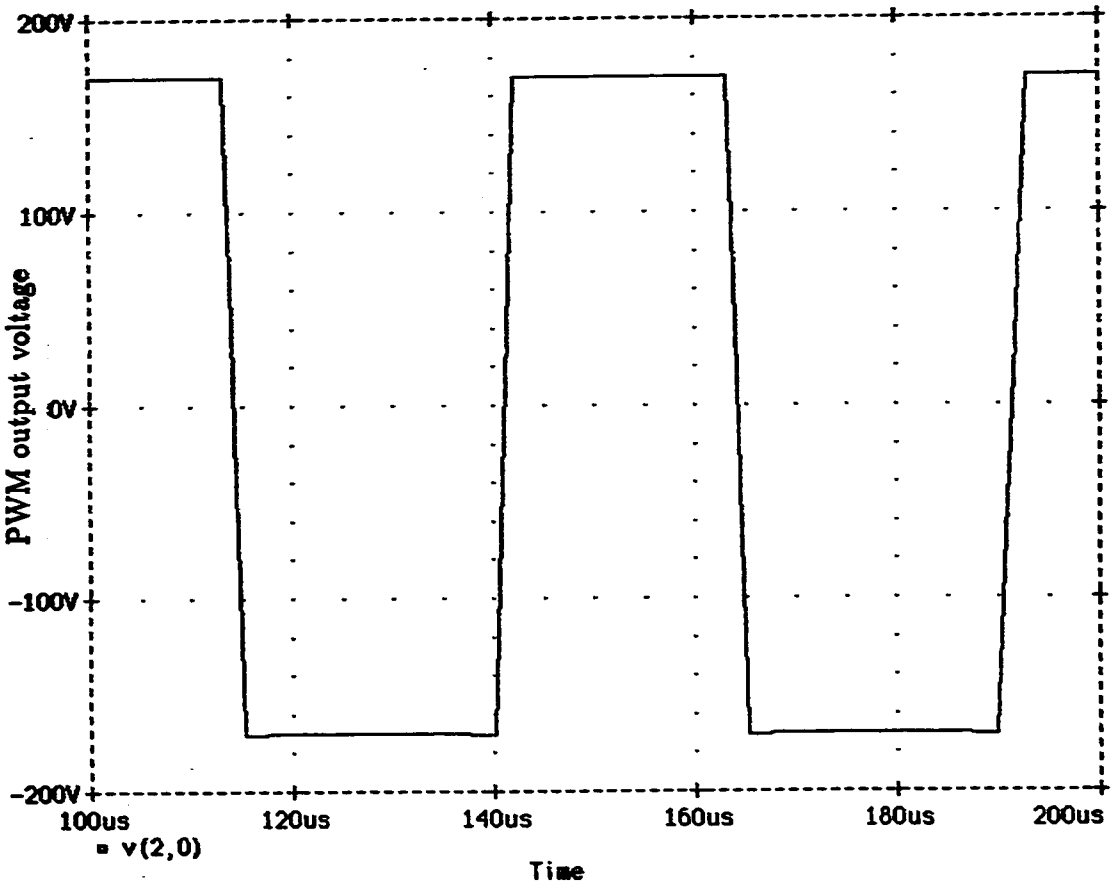


Figure 4.16: Out put PWM for IRF250

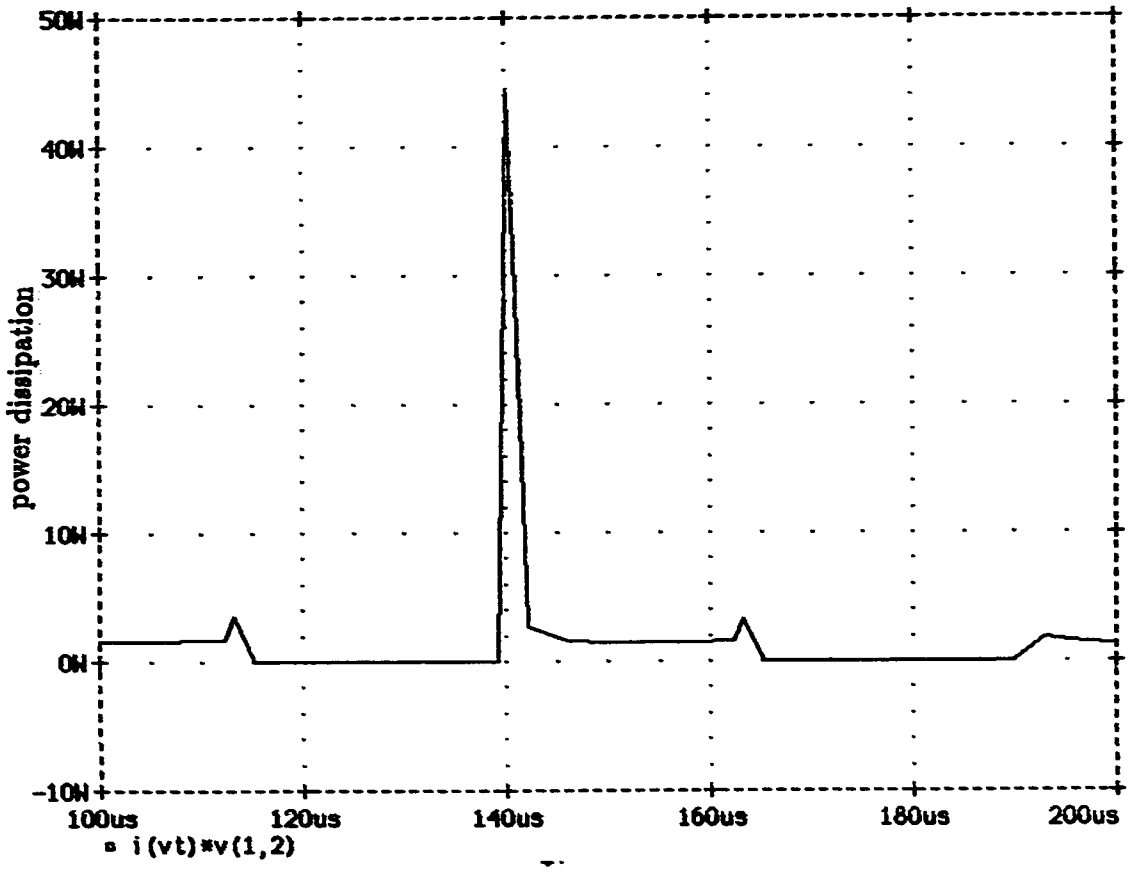


Figure 4.17: Instantaneous power dissipation for IRF250 bridge

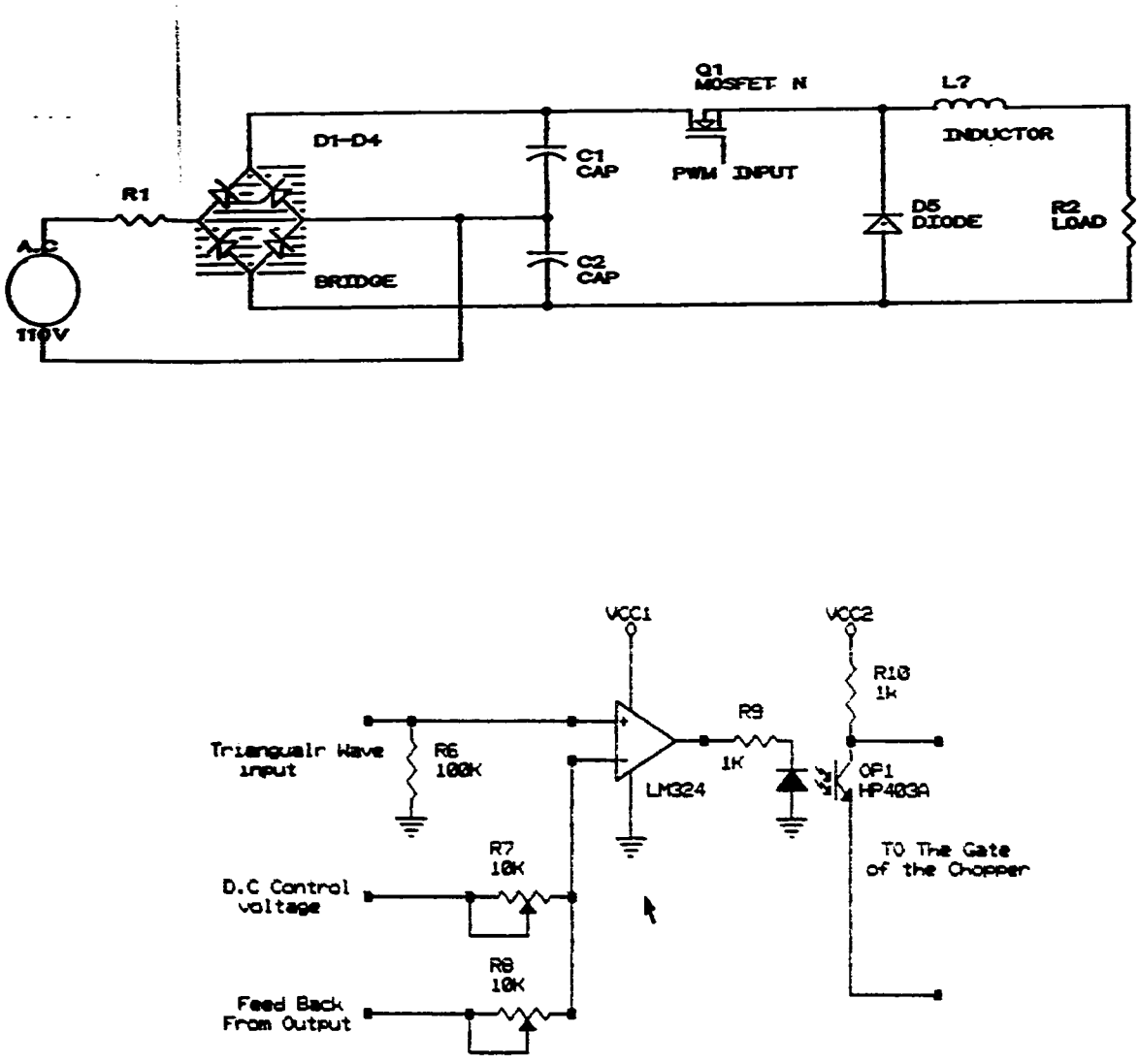


Figure 4.18: Circuit diagram of doubler and charger section

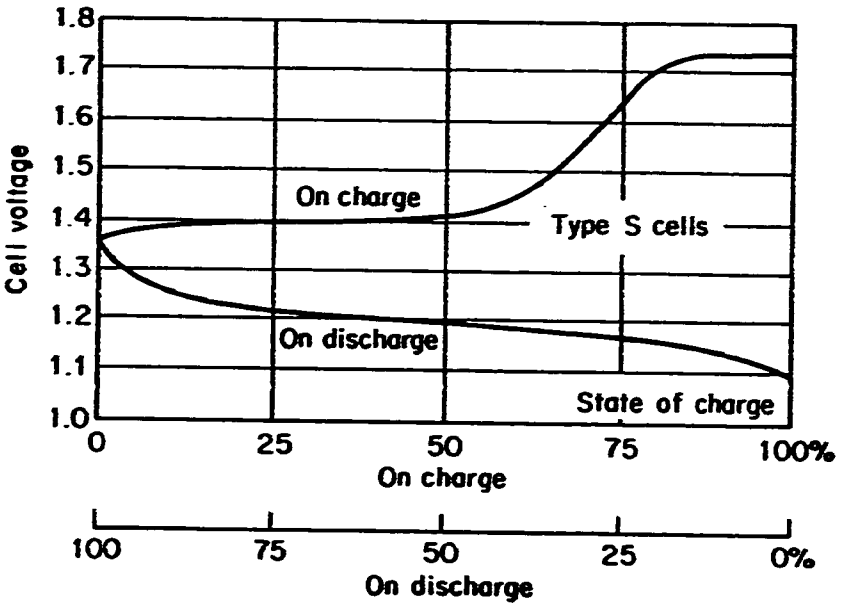


Figure 4.19: Charge discharge curves for nicad batteries

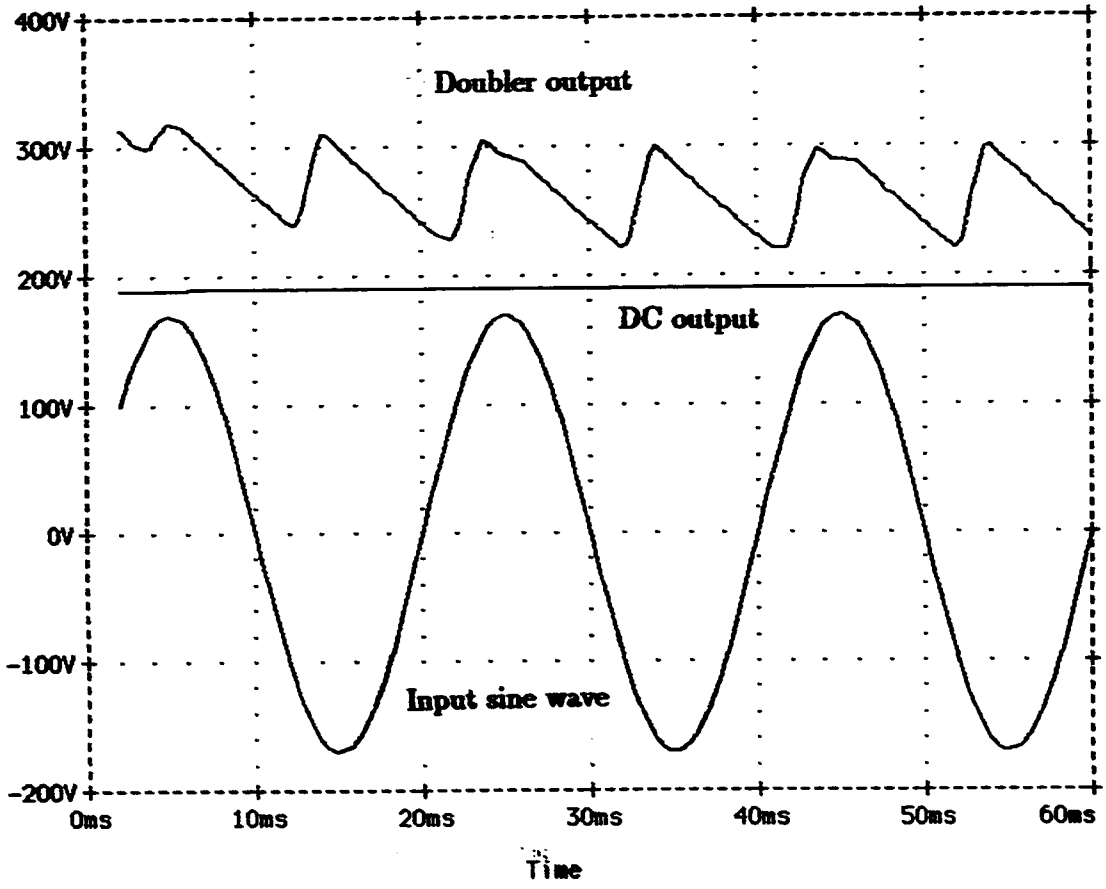


Figure 4.20: Doubler and battery charge section output

Chapter 5

IMPLEMENTATION AND SIMULATION: RESULTS

It is a general trend now a days that most of the *designers simulate their circuits on a computer* before doing any breadboarding in order to save time and to avoid initial damage of the power components. This becomes even more *critical when designing the expensive and high power circuits.* The advancements in microcomputers have made simulation programs available at a low cost, and running them on high performance IBM PC, PS or MACs helps in efficient design.

This chapter describes the laboratory implementation of the various building blocks of the UPS. A novel method for digital feedback simulation has been tested. The digital as well as analog feed back techniques are discussed. UPSs employing both these techniques are simulated. The output of the UPS under varying load conditions has been shown. Inverter has been simulated using VDMOS as the switching element. The last section deals with the monitoring and the diagnostics techniques

for the UPS.

5.1 Laboratory Implementation

5.1.1 Doubler/Battery Charger

Doubler and battery charger section was practically implemented. The results obtained were same as obtained by the simulation. Figure 5.1 show the output of the doubler section. This output is the input for the chopper. The chopper was operated at a frequency of approxiamately 1Khz. Complete circuit of the doubler/battery charger section is shown in figure 4.18. The results of changing the pulse widths on the D.C output are shown in the figure 5.2 and figure 5.3.

5.1.2 Inverter Section

PWM generator, base driver, inverter and the filter section were practically implemented in the laboratory. Natural sampling strategy was used for the generation of PWM. Figure 5.4 show the comparison of a reference sine wave and the carrier traingular waveform. The PWM produced as the result of the comparison can be seen in the figure 5.5. The PWM Thus produced was applied to the base driver circuit. Isolation was achieved by the use of opto-isolators. Inverter section consisted of four IRF630 MOSFETS connected in the standard full bridge configuaration. The output of the inverter was applied to the simple LC low pass filter. The value of inductor was 16.4mh and filter capacitor was 100uf. Complete circuit of the inverter/filter section is shown in figure 5.6. figure 5.7 and figure 5.8 show the PWM which is produced by the inverter and the sine wave that is obtained at the output

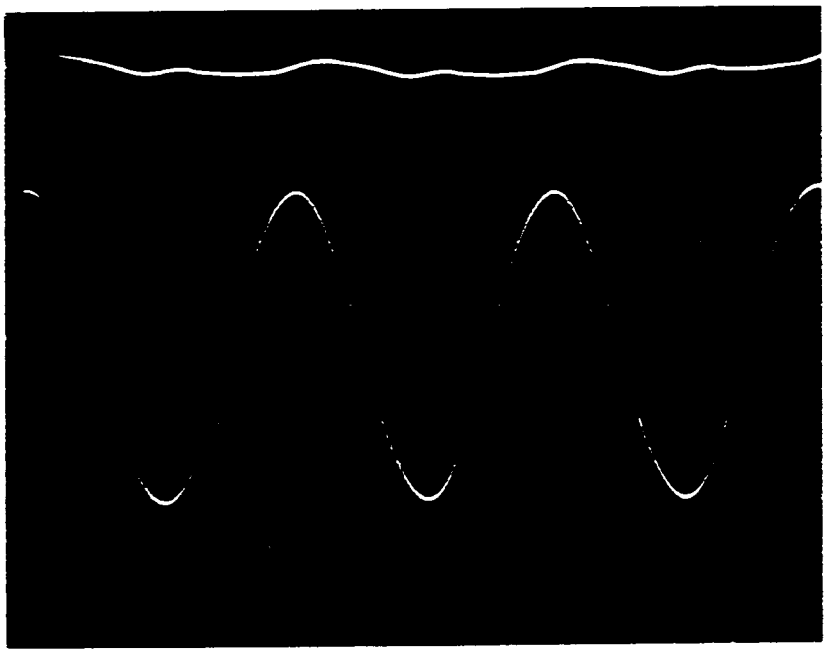
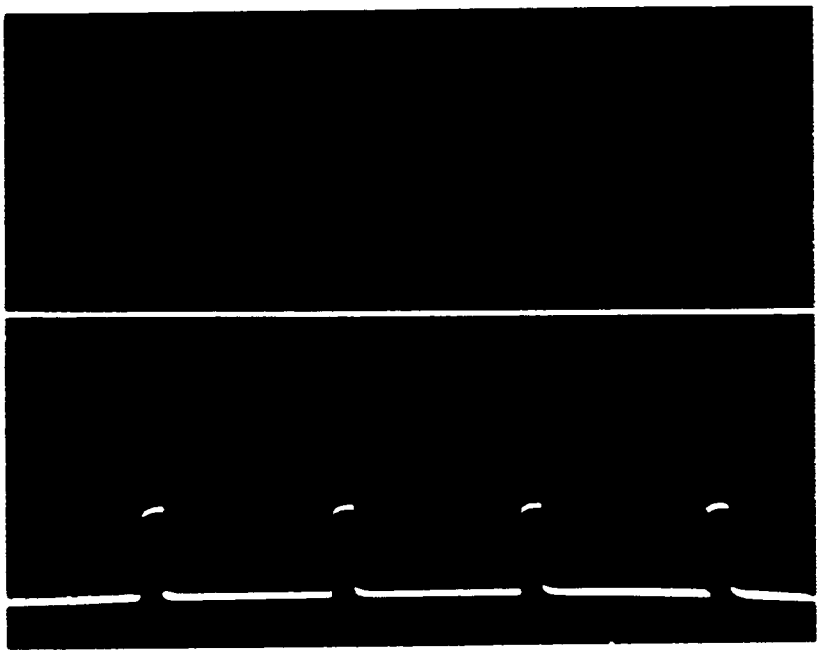
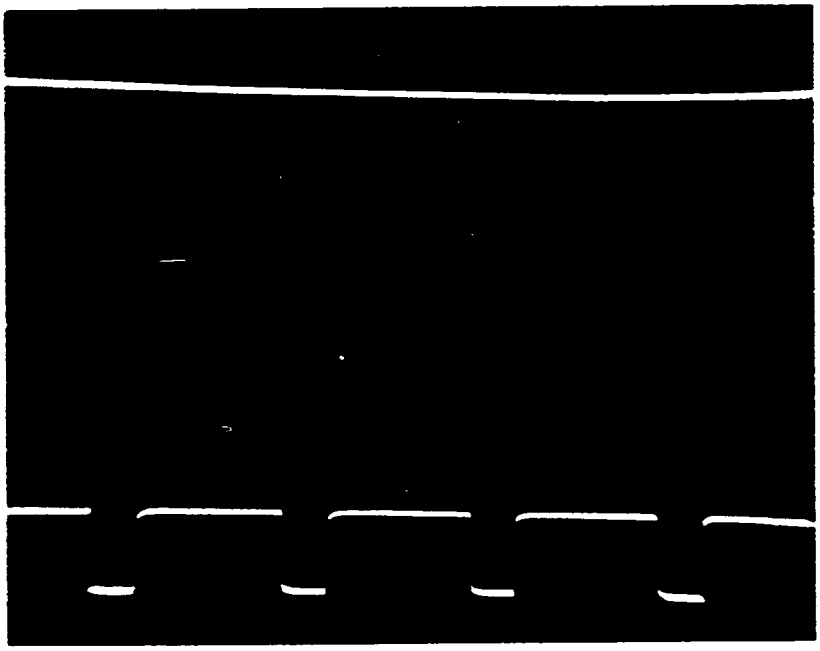


Figure 5.1: Input and the output of doubler section: Upper Trace; 10V/DIV;5ms/DIV : Lower Trace; 10V/DIV



Upper trace: Filtered DC ; Lower trace: Control voltage

Figure 5.2: Small pulse-width produces less D.C vloltage: Upper Trace; 10V/DIV;0.5ms/DIV : Lower Trace; 10V/DIV



Upper trace: Filtered DC ; Lower trace: Control voltage

Figure 5.3: Large pulse-width produces higher D.C voltage: Upper Trace; 10V/DIV;0.5ms/DIV : Lower Trace; 10V/DIV

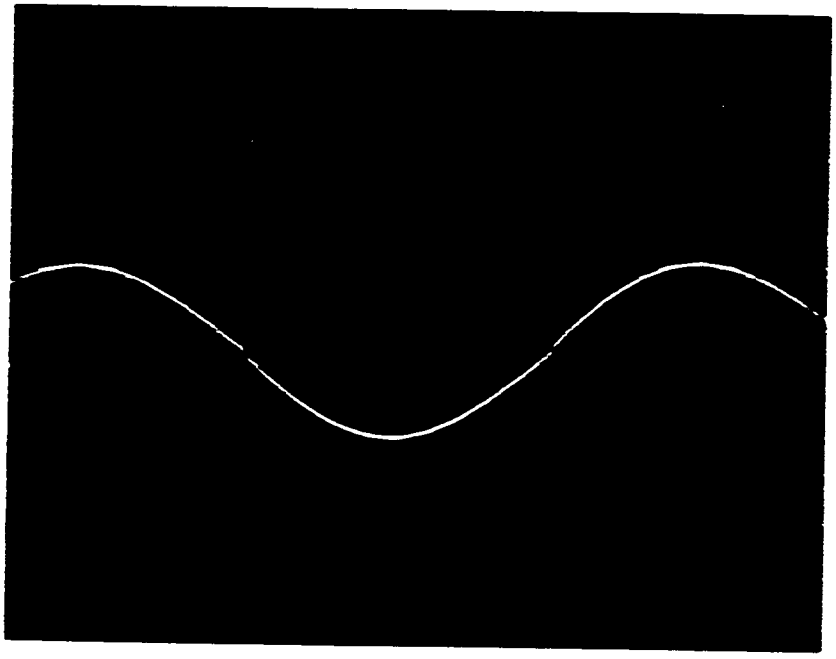


Figure 5.4: Reference sine wave and carrier triangular waveform : Upper Trace; 5V/DIV;2ms/DIV : Lower Trace; 5V/DIV

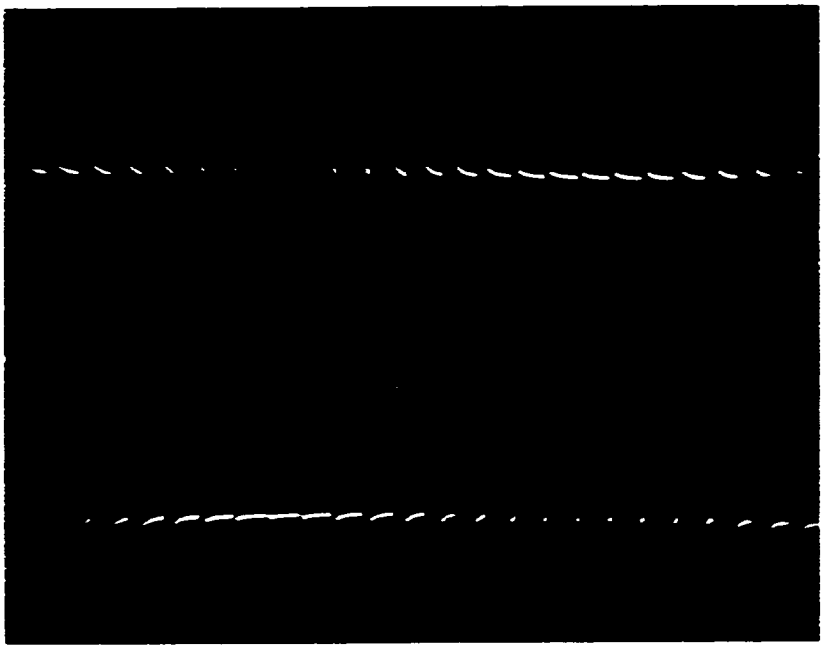


Figure 5.5: Resultant PWM waveform: Upper Trace; 5V/DIV;2ms/DIV : Lower Trace; 5V/DIV

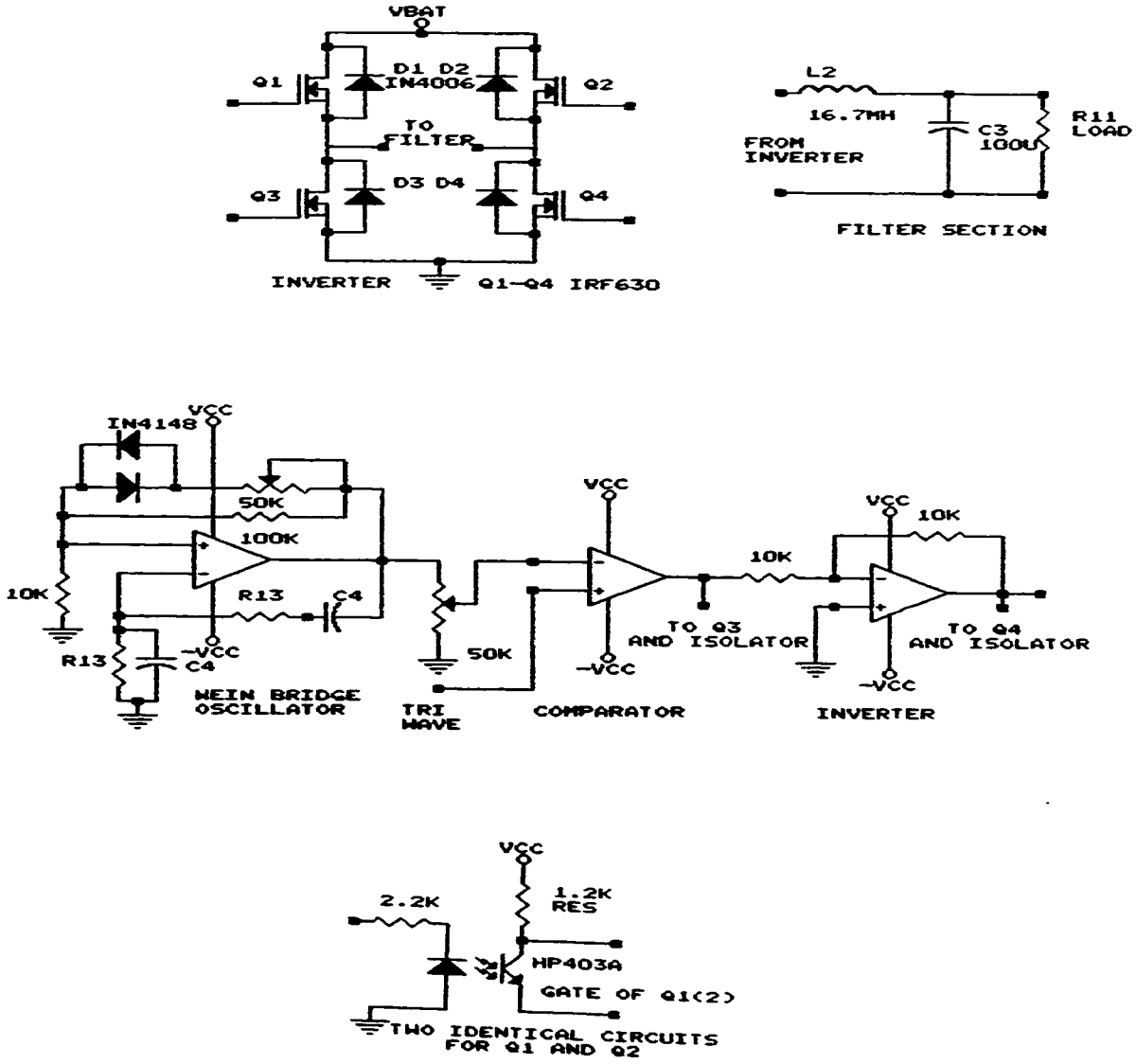


Figure 5.6: Inverter/filter section along with control circuitry

of the LC filter for different index of modulation. It is evident that the quality of the output waveform is excellent. Moreover it can be clearly seen that changing the modulation index effectively controls the amplitude of the output waveform.

The effect of reducing the filter capacitor(10uf) is illustrated in figure 5.9 and figure 5.10 for different index of modulation. It can be clearly seen that that ripple content in the output waveform is increased when the filteration is poor.

5.1.3 Putting it Together

Doubler, battery charger, Inverter, and the filter section were connected together. Natural sampled PWM was applied to the gates of the inverter. Whereas chopper was controlled by changing the duty cycle of 1 KHz carrier. The input sine wave and the waveform that we get at the output of the filter are shown on the next pages. figure 5.11 show the input and the output waveforms for the UPS employing good filteration(filteration capacitor 100uf). figure 5.12 show the input and the output waveforms when the filteration is reduced(filteration capacitor 10uf).

5.2 FEEDBACK CIRCUITRY

The feedback circuity is utilized to convert the output voltages into digital signals and to feed these into the microcomputer to implement the closed loop control system. In analog feedback the output voltage is fed back to a comparator which controls the modulation index of the natural sampled PWM. The simulation of both type of feedback will be discussed.

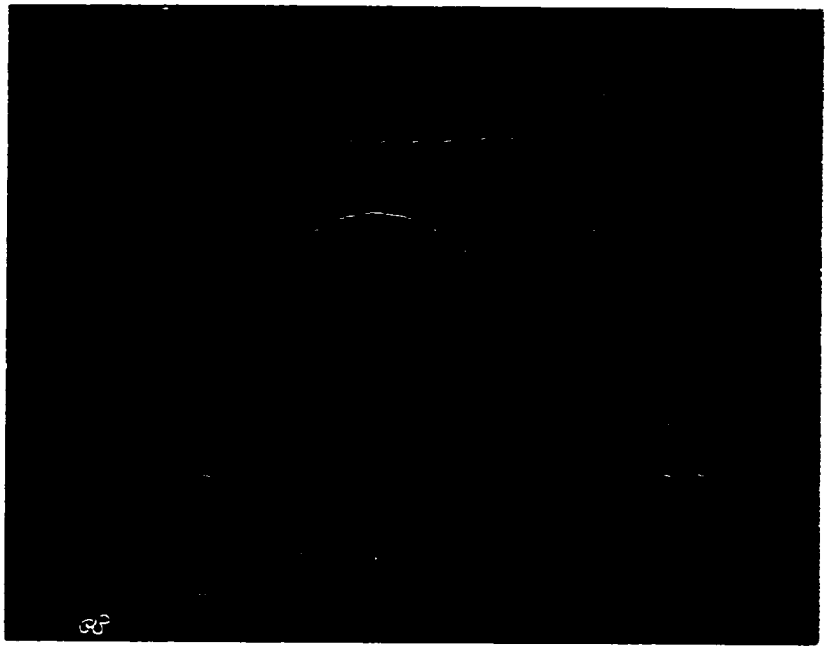


Figure 5.7: PWM and the resultant sine wave for lower modulation index: Upper Trace; 10V/DIV;2ms/DIV : Lower Trace; 10V/DIV

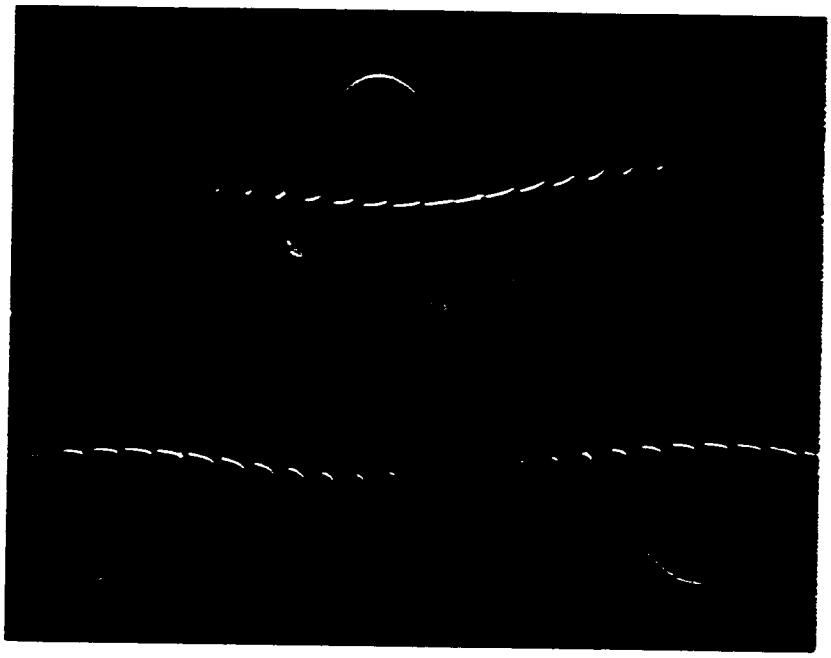


Figure 5.8: PWM and the resultant sinewave for higher modulation of index: Upper Trace; 10V/DIV;2ms/DIV : Lower Trace; 10V/DIV

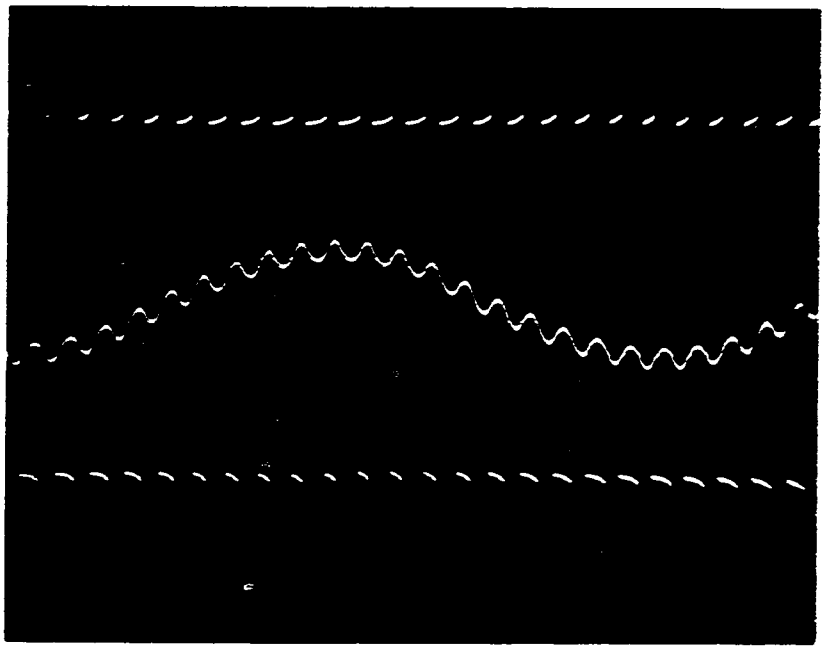


Figure 5.9: PWM and the resultant sinewave with less filteration and lower index of modulation: Upper Trace; 10V/DIV;2ms/DIV : Lower Trace; 10V/DIV

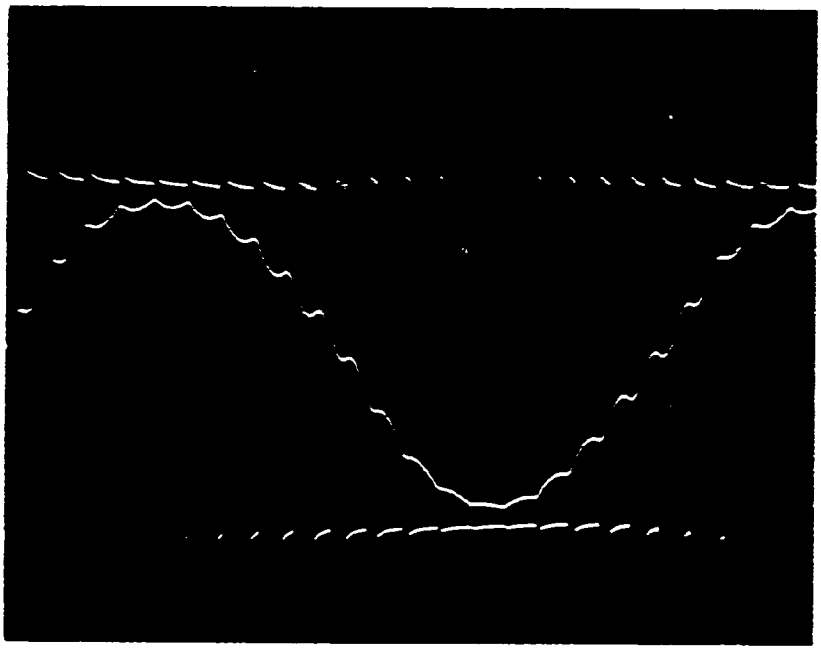


Figure 5.10: PWM and the resultant sinewave with less filteration and higher index of modulation: Upper Trace; 10V/DIV;2ms/DIV : Lower Trace; 10V/DIV

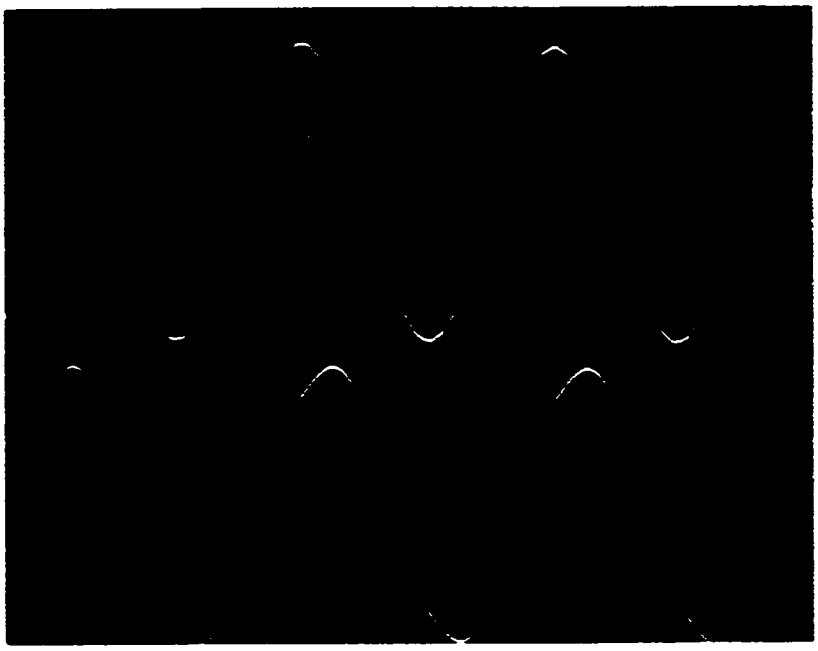


Figure 5.11: Input and output waveforms for the UPS with good filteration: Upper Trace; 10V/DIV;5ms/DIV : Lower Trace; 10V/DIV

Figure 5.12: Input and output waveforms for the UPS with reduced filteration: Upper Trace; 10V/DIV;5ms/DIV : Lower Trace; 10V/DIV

5.2.1 Simulation and Implementation of Analog Feedback

In the actual implementation utilizing analog feedback technique the output voltage is stepped down, then compared with the reference signal and an error signal generated. This error signal is then used to control the modulation index of the natural sampled PWM. This controls the amplitude of the output voltage. As SPICE can support analog feedback, therefore the above mentioned procedure was used. The PSPICE listing for testing the analog feedback is shown in appendix A.2. The output taken from the filter was compared with a reference signal the error signal controlled the modulation index of the natural sampled PWM. This effectively controls the amplitude of the of the out put sine wave signal. The output of an inverter utilizing analog feedback is shown in the figure 5.13 for normal load. Figure 5.14 and figure 5.15 show the output when the load is doubled and the load is halved respectively.

5.2.2 Simulation and Implementation of Digital Feedback

In case of a digital control the output voltage is stepped down to a low level. This voltage is then applied to the A/D converter (a sample and hold circuit is utilized to provide constant voltage during the A/D conversion process), which feeds this digital signal to the microcontroller or a microprocessor. Depending on the level of the digital signal, the microprocessor calculates the appropriate pulse width to maintain the output voltage constant.

SPICE has no provision to implement digital feedback, so to simulate the UPS utilizing digital feed back a special technique was used. The main features of this

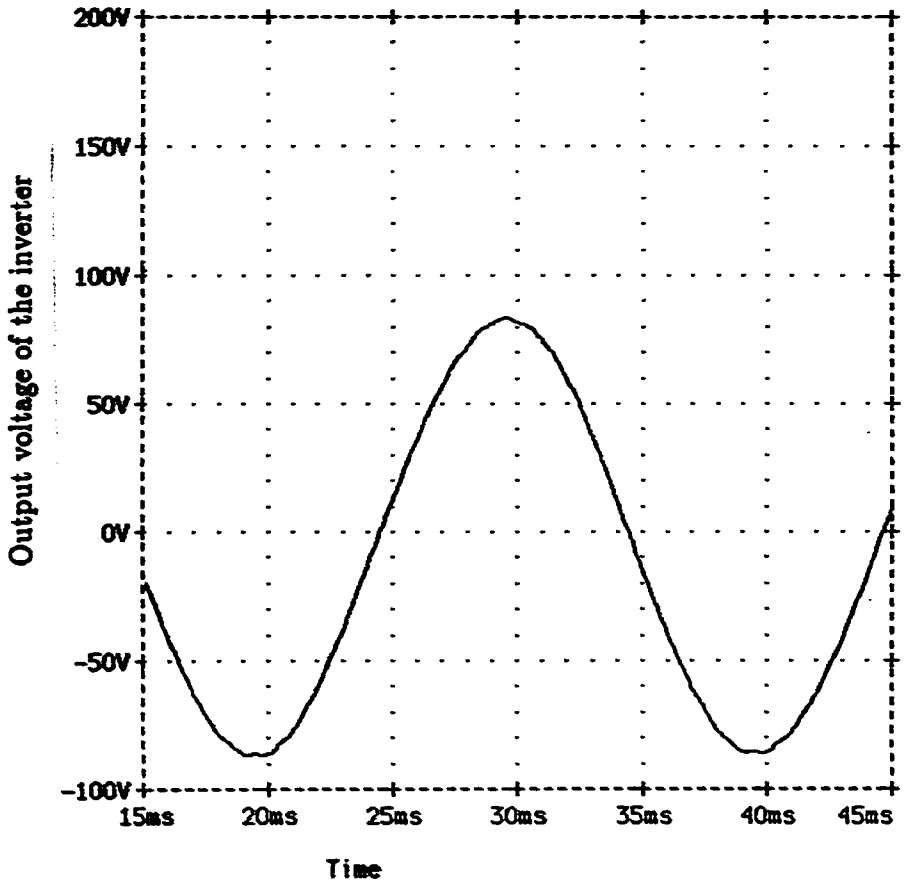


Figure 5.13: Inverter output at normal load

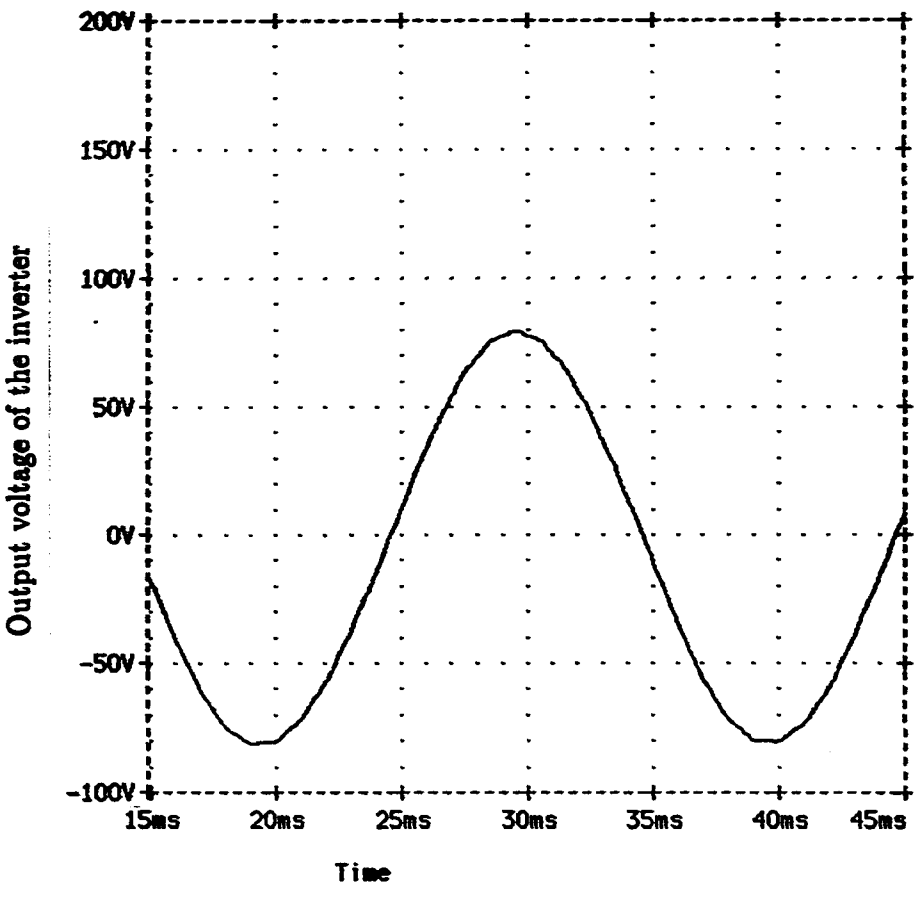


Figure 5.14: Inverter output at double load

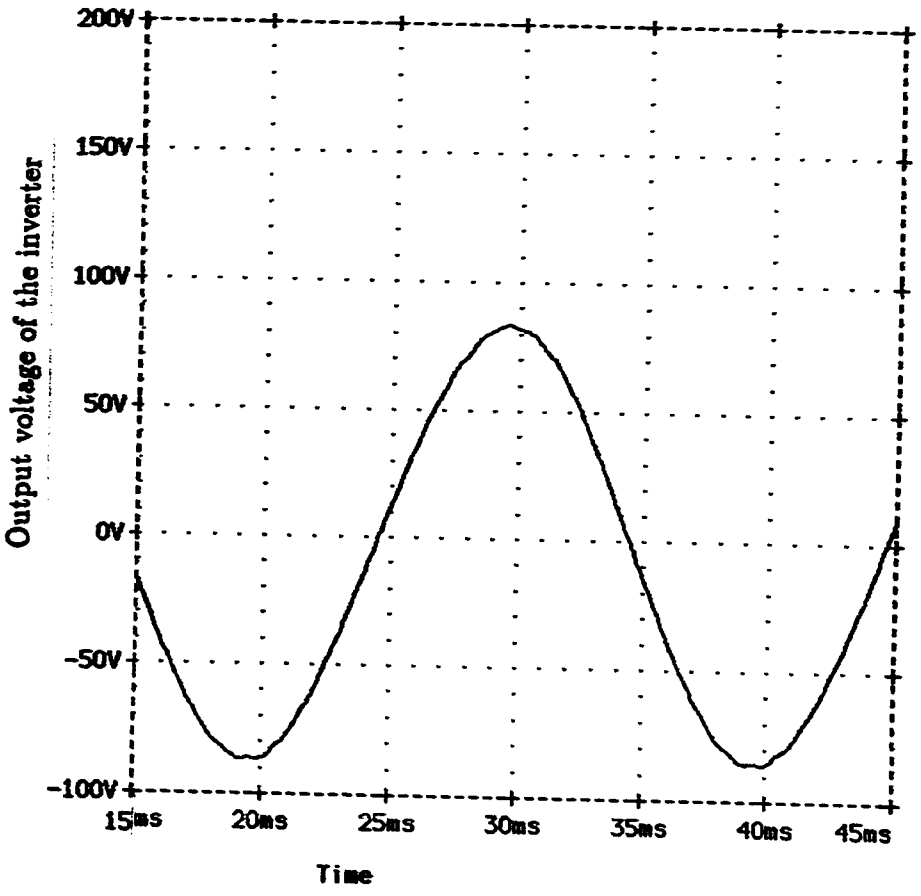


Figure 5.15: Inverter output at half load

scheme are as follows.

- The pulse widths T_{HAj} for a quarter of a cycle and for different modulation indices (from .75 to .975 in .005 step) were calculated before hand and were stored in the file as a lookup table.
- The *.cir program is run for a single pulse.
- The outputs from *.cir are stored in another file.
- The output is read and a new pulse width is put in the *.cir file for the next run.
- The new pulse width which is put, depends on the output voltage from the previous run.
- The various node voltage and currents are put in the *.cir file as initial conditions for the next run.
- The above steps are repeated to complete the required analysis.

The PSPICE listing for digital feedback simulation is shown in appendix A.1. Programs were developed in assembly and turbo basic for look-up table generation, calculating pulse widths for different instants, and manipulating the data in various files. These programs are given in appendix B.3, B.2 and B.1 respectively. The output of a UPS using digital feed back is shown in figure 5.16 and figure 4.2 for full load and half load respectively.

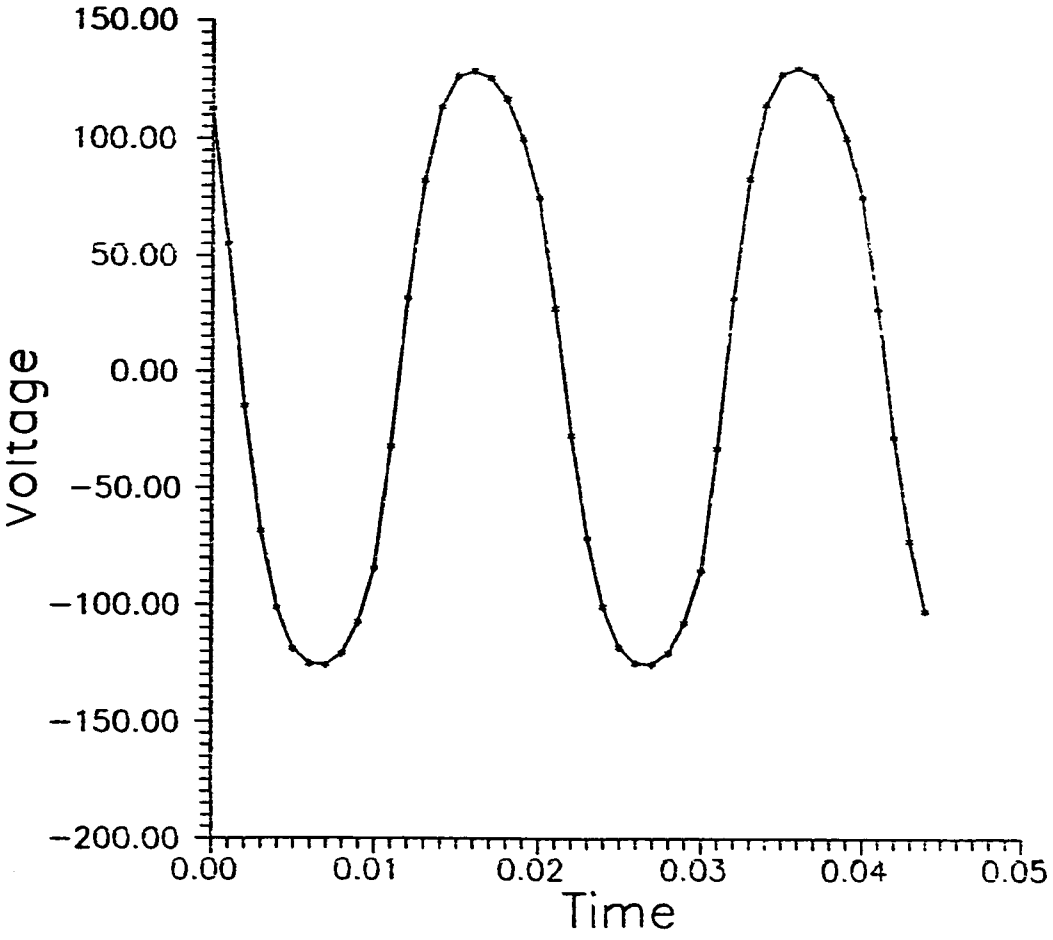


Figure 5.16: Output of inverter using digital feedback

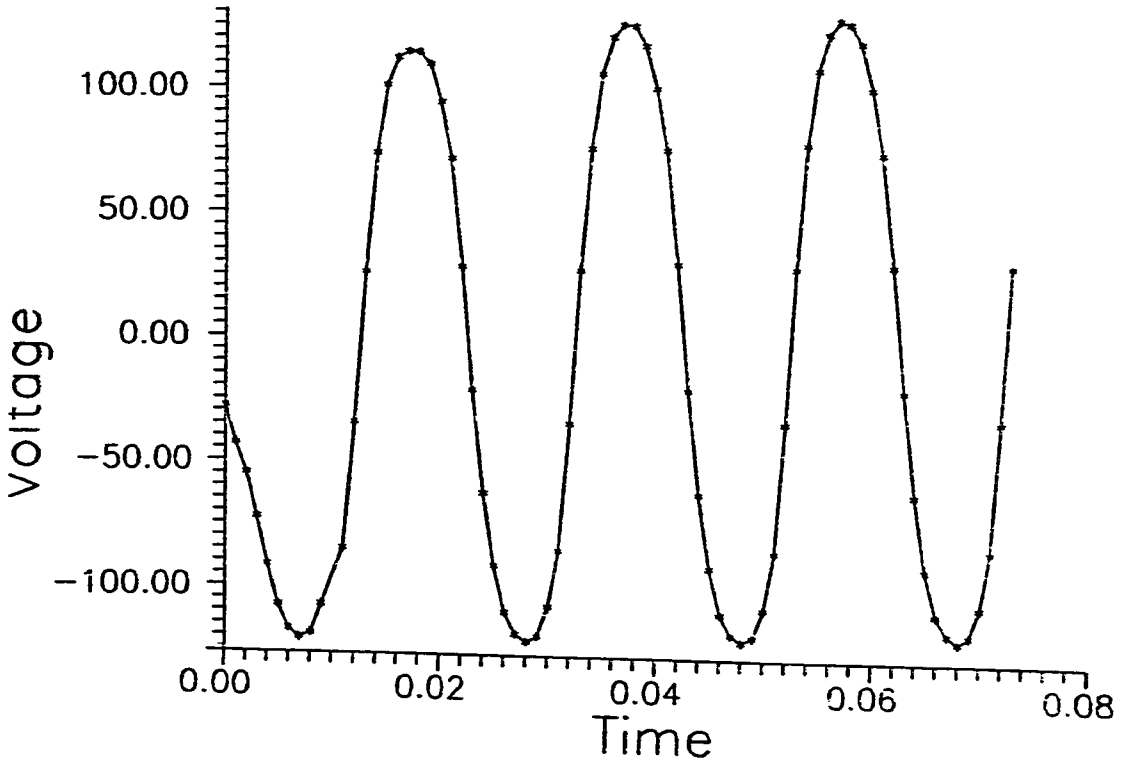


Figure 5.17: Output when load is halfed

5.3 Monitoring and Diagnostics

An uninterruptible power supply has the task of improving the reliability of the power supply to load. In addition to the actual design the factors such as reduced down times contribute to assuring the reliability of these power supply systems, particularly in important installations [25]. That is why it is necessary not only to have the stock of critical spare parts but also to analyze faults precisely and comprehensively. Although this task is performed by the service personnel. Use of microprocessor can help in keeping the record of the equipment status, which can be of great help to the service personnel when a fault occurs. Monitoring of the voltage and frequency may help to transfer the load to other source when UPS malfunctions. In the next section static transfer switches, and voltage and frequency monitoring techniques will be discussed.

5.3.1 Static Transfer Switches

Static Transfer Switches are normally employed for the uninterruptible transfer of load to an alternative source in case of any abnormalities in voltage and frequency, or in case if UPS inverter starts malfunctioning. Standard UPSs are equipped with two power SCRs connected antiparallel in series with the load as shown in figure.

These can transfer the load between the inverter output and the alternative power source fast enough to accomplish a "no break" in power during transition. Use of static transfer switches in the actual design is recommended.

5.3.2 Voltage Monitoring Techniques

UPSs using PWM inverters are switched at higher frequencies than the required output frequency. This enables the harmonics of the switching frequency and its side bands to be filtered out with the use of low pass filters having small inductors and capacitors (instead of filters tuned to 60Hz fundamental frequency) and which endows the system with fast transient response. Small filtering components are liable to store rather less energy, thus necessiating the need for fast detection of disturbances.

The most simple voltage sensing method is based on the comparison of the output signal and DC reference signal. The resulting error is integrated. This method suffer from integration delays which cannot be tolerated for quick detection. Another method reported in the literature is by [26], in this method the output waveform is constantly compared with a phase-locked reference sine wave. This technique produces quite acceptable results. It may be employed successfully in the actual design.

5.3.3 Frequency Monitoring Techniques

In order to protect the critical loads from excessive frequency variations, a frequency measurement technique equipped with fast response is required. Some loads may or may not be sensitive to frequency instability; switching power supplies can accept a wide frequency variation whilst some CRT displays demand $50Hz \pm 0.01\%$. The rate of change of frequency is especially important for installations employing motors. A sudden change in frequency could result in an unacceptable high inrush current to

the motor. Consequently, the maximum slew rate allowed for most critical loads is about 0.5Hz/s. Some techniques are described in the literature [27] for minimum maximum frequency indication. They rely on the period measurement technique. It can be effectively employed to monitor the frequency of the actual working circuit.

5.3.4 Simulation

In simulation the value of voltage and current at different nodes is written to a file tst.str at the end of each carrier period. These values can be read afterwards for diagnostic purposes or may be transmitted to a central station.

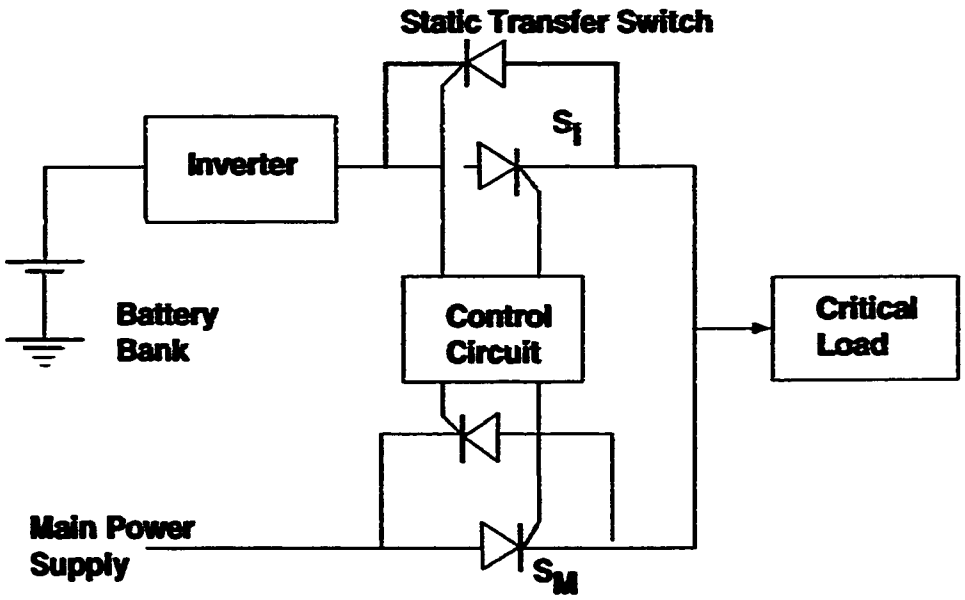


Figure 5.18: UPS with static transfer switch

Chapter 6

CONCLUSIONS AND SUGGESTIONS FOR FURTHER WORK

This chapter presents the conclusions arising from the results described in the previous chapters and gives suggestions for further research work.

6.1 Conclusions

The results obtained from the simulation of regular sampled PWM suggests that it is advantageous to use this strategy for the design of microcontroller based UPS system. Look-up-table method overcomes the time consuming job of calculating pulse widths for each cycle. Since The PWM generation technique effectively provides equal segmentation of the output waveform, the total number of segments in a cycle are equal to the ratio of the carrier frequency to the modulating frequency. The

carrier frequency was 20KHz and the ratio was 400. The use of ultrasonic carrier frequency made the whole system compact and noiseless.

Two equations, Eqns. 3.7 and 3.12, are derived to calculate the low level pulses for the double-edge and single-edge modulation processes respectively using the regular sampled symmetric strategy. Eqn. 3.7 requires less computation time as compared to other equations available to date in the literature for performing the same task.

The use of VDMOS and their simple drive circuitry in the UPS inverter allow these to be designed using high frequency carrier signals, resulting in high quality output voltage waveforms. The use of 20Khz switching frequency provides the means of simplifying the design of the microprocessor controlled PWM generators, and allows the use of simple low pass output filters.

This UPS doesn't contain input and output transformers as found in the conventional UPS' s. Input transformer was eliminated by the implementation of chopper / doubler section and by the use of high voltage battery bank. This also eliminated the need for bulky output transformer. the size of output filters was reduced considerably by the use of ultrasonic carrier frequency.

The UPS was designed and simulated. Certain portions of the UPS were implemented in the lab. Since SPICE doesn't support VDMOS model, a model was developed and was used in the simulation. Another limitation with SPICE is that it doesn't provide digital feedback simulation. A unique method for the simulation of

regular sampled PWM and digital feedback was developed. This allowed the simulation of the complete UPS. The results obtained from the practical implementation are presented in chapter four. Whereas, simulation results are given in chapters four and five.

Electrical isolation between the control circuitry and the gate drive system was realized by the use of opto-isolators. These were found to facilitate a good interface to the pulse generating system.

6.2 Suggestions for Further Research Work

The remaining portion of the UPS (Microcontroller Based System) should be practically implemented. Use of 8096 microcontroller is suggested. It has built-in programmable counters and A/D converter. Counters after being loaded by a appropriate value from the look-up-table can be used for the generation of PWM. The presence of A/D converter on the 8096 chip will facilitate the implementation of feed back and voltage monitoring schemes.

New switching devices such as Insulated Gate Bipolar Transistors (IGBTs) or Silicon Induction Transistors (SIT) may be tried in place of VDMOS and the results compared to the original design.

Some good methods of device protection should be implemented. The problem of current "Shoot-Through" should be solved by using the software techniques ensuring that no device switch on until its complement has been switched off. Hall

effect sensors can be used to detect the current passing from the D.C supply side to the inverter. The protection circuit should detect the rate of rise current.

The present design may be extended to three phase UPS with the feedback from each phase. This will provide instant control over output voltage waveform, thus enabling unbalanced loads to be properly dealt with.

Appendix A

Spice Program Listings

A.1 A Program to Test Digital Feedback Circuit

```
TO TEST DIGITAL FEED BACK
VTST   13  0   PWL(0 -10 20NS 10 25.00US 10 25.02US -10)
LF      2  4  30MH  IC=00.00A
CF      4  0  40UF  IC=00.00V
RL      4  0  20
VS1     1  0  170V
VS2     0  3  170V
EPW1    6  3  13  0  1
RTST 13  0  100K
EPW2    5  2  0  13 1
X2      1  5  2  MTH5N100
X4 2  6  3  MTH5N100
D3      3  2  DMOD
D4     2  1  DMOD
.MODEL  DMOD D (RS=0.3)
.TRAN  25US  50US  UIC
.OPT ITL5=0  RELTOL=.01
.OPT LIMPTS=501
.PRINT TRAN V(4,0) I(LF)

*BEGINNING OF THE SUBCIRCUIT FOR VDMOS
.SUBCKT  MTH5N100  20  10  30
RG  10  1  5
M1  2  1  3  3  DMOS  L=1U  W=1U
```

```
.MODEL  DMOS  NMOS  (VTO=3.36 KP=3.73 LEVEL=1)
CGS  1  3  1642P
RD  20  4  1.27
DDS  3  4  DDS
.MODEL  DDS  D (BV=1000 M=0.48 CJO=873P VJ=0.43)
DBODY  3  20  DBODY
.MODEL  DBODY D (BV=1000  IS=3.6E-11  M=1.03 RS=0.57 TT=1U)
RA  4  2  1E-3
RS  3  5  1M
LS  5  30 8M
M2  1  8  6  6  INTER
E2  8  6  4  1  2
.MODEL INTER NMOS (VTO=0 KP=10 LEVEL=1)
CGDMAX  7  4  7500P
RSGD  7  4  1E7
DGD  6  4  DGD
RDGD  4  6  1E7
.MODEL DGD  D (M=0.5 CJO=7500P VJ=0.00337)
M3  7  9  1  1  INTER
E3  9  1  4  1  -2
.ENDS MTH5N100
.END
```

A.2 A Program to Test Analog Feedback

```
CIRCUIT TO TEST VDMOS IMPLEMENTED BRIDGE WITH PWM INPUT AND FEED BACK
*BEGINNING OF THE SUBCIRCUIT FOR PWM GENERATOR

.SUBCKT  PWMG 42  43  47
VTRI  41 47  PULSE(-10 10 0  24.5US  24.5US  1US 50US)
*VSIN  42  47  SIN(0  8  50)
RIN   41 42  10K
D1    44  43  D1N758
D2     44  47  D1N758
RL     45  43  1MEG
.MODEL  D1N758 D (IS=0.05UA RS=0 BV=9.49V )
EPWM  45  47  41  42  1000
.ENDS PWMG

*BEGINNING OF THE SUBCIRCUIT FOR VDMOS
.SUBCKT  MTH5N100  20  10  30
RG  10  1  5
M1  2  1  3  3  DMOS  L=1U  W=1U
.MODEL  DMOS  NMOS  (VTO=3.36 KP=3.73 LEVEL=1)
CGS  1  3  1642P
RD  20  4  1.27
DDS  3  4  DDS
.MODEL  DDS  D (BV=1000 M=0.48 CJO=873P VJ=0.43)
DBODY  3  20  DBODY
```

```
.MODEL  DBODY D (BV=1000  IS=3.6E-11  N=1.03 RS=0.57 TT=1U)
RA  4  2  1E-3
RS  3  5  1M
LS  5  30 8N
M2  1  8  6  6  INTER
E2  8  6  4  1  2
.MODEL INTER NMOS (VTO=0 KP=10 LEVEL=1)
CGDMAX  7  4  7500P
RSGD  7  4  1E7
DGD  6  4  DGD
RDGD  4  6  1E7
.MODEL DGD  D (M=0.5 CJO=7500P VJ=0.00337)
M3  7  9  1  1  INTER
E3  9  1  4  1  -2
.ENDS MTH5N100

*BEGINNING OF THE MAIN CIRCUIT
XS1     12  13  0  PWMG
*XS3     12  11  0  PWMG
*RS1     13   0  100MEG
*RS3     11   0  100MEG
VS1     1  0  170V
VS2     0  3  170V
EPW1    6  3  13  0  1
*VTST   6  3  PULSE(-10 10 0 .495MS .494MS 10US 1MS)
EPW2    5  2  0  13 1
```

```
X2      1  5  2  MTH5M100
X4 2  6  3  MTH5M100
D3      3  2  DMOD
D4     2  1  DMOD
.MODEL  DMOD D (RS=0.3)
RL      4  0  40
LF      2  4  30MH
CF      4  0  40UF
ESIN 12 0 POLY(2) 9,0  4,0  0  1  -.01
VSIN   9  0  SIN(0  8  50)
RSIN 9  0  100K
.TRAN  .5MS  50M
.OPT ITL5=0  RELTOL=.01  ITL4=500
.OPT LIMPTS=501
.PRINT TRAN V(4)
.PLOT TRAN V(4)
.END
```

A.3 MOS Bridge and the Driver Circuit Without Feedback

```
CIRCUIT TO TEST MOS IMPLEMENTED BRIDGE WITH PWM INPUT
.SUBCKT  PWMG  3  7
VTRI  1  7  PULSE(-10 10 0  .495MS  .495MS  10US 1MS)
VSIN  2  7  SIN(0  8  50)
RIN   1  2  10K
D1    4  3  D1N758
D2    4  7  D1N758
RL    5  3  1MEG
.MODEL  D1N758 D (IS=0.05UA RS=0 BV=9.49V )
EPWM  5  7  1  2  1000
.ENDS PWMG
XS1     10  2  PWMG
XS3     11  3  PWMG
VS1     1  0  170V
VS2     0  3  170V
EPW1    6  3  11  3  1
*VTST   6  3  PULSE(-10 10 0 .495MS .494MS 10US 1MS)
EPW2    5  2  2  10 1
M1      1  5  2  2  NMOD
M2      2  6  3  3  NMOD
.MODEL NMOD NMOS (VTO=3.32 KP=5.5  CGSO=2540 CGDO=160PF THETA= 0.058  LEVEL=1)
D3      3  2  DMOD
D4     2  1  DMOD
```

```
.MODEL  DMOD D (RS=0.3)
RL      4  0  20
LF      2  4  30MH
CF      4  0  40UF
.TRAN  10US 45M  20M
.OPTIONS ITL5=0  RELTOL=.01
.PROBE
.END
```

A.4 Doubler With MOSFET in the Chopper Stage

```
SECOND TYPE OF DOUBLER CIRCUIT FOR UPS
VIN 1  0  SIN(0  170  50)
R8  1  2  .001
R9  0  3  .001
C2  2  3  0.001UF
C1  5  3  6800UF   IC=170V
C3  3  4  8000UF   IC=170V
D1  2  5  DMDL
D2  4  2  DMDL
D3  4  8  DMDL
.MODEL  DMDL  D(VJ=0.7  BV=600)
M1  5  7  8  8 QMDL
.MODEL  QMDL  NMOS(VTO=3.6048 KP=13.44 LAMBDA=0 RS=.1293 PB=1 RD=.7577 LEVEL=1)
L7  8  9  100MH
RL  9  4  10
RPW 7  10  47
CBAT  10  4  10000UF     IC=200V
RBAT  9   10  0.1
VPW  10  8  PULSE(0  10  0  .1MS  .1MS  0.8MS  2MS)
.OPT  ITL5=0  RELTOL=.01
.TRAN  1M  60M  2M  UIC
.PROBE
.END
```

A.5 Doubler With VDMOS in the Chopper Stage

```
SECOND TYPE OF DOUBLER CIRCUIT FOR UPS
VIN 1  0  SIN(0  170  50)
R8  1  2  .001
R9  0  3  .001
C2  2  3  0.001UF
C1  5  3  6800UF   IC=170V
C3  3  4  8000UF   IC=170V
D1  2  5  DMDL
D2  4  2  DMDL
D3  4  8  DMDL
.MODEL  DMDL  D(VJ=0.7  BV=600)
X1  5  7  8   MTH5N100
*BEGINNING OF THE SUBCIRCUIT FOR VDMOS
.SUBCKT  MTH5N100  20  10  30
RG  10  1  5
M1  2  1  3  3  DMOS  L=1U  W=1U
.MODEL  DMOS  NMOS  (VTO=3.36 KP=3.73 LEVEL=1)
CGS  1  3  1642P
RD  20  4  1.27
DDS  3  4  DDS
.MODEL  DDS  D (BV=1000 M=0.48 CJO=873P VJ=0.43)
DBODY  3  20  DBODY
.MODEL  DBODY D (BV=1000  IS=3.6E-11  N=1.03 RS=0.57 TT=1U)
RA  4  2  1E-3
```

```
RS  3  5  1M
LS  5  30 8N
M2  1  8  6  6  INTER
E2  8  6  4  1  2
.MODEL INTER NMOS (VTO=0 KP=10 LEVEL=1)
CGDMAX  7  4  7500P
RSGD  7  4  1E7
DGD  6  4  DGD
RDGD  4  6  1E7
.MODEL DGD  D (M=0.5 CJO=7500P VJ=0.00337)
M3  7  9  1  1  INTER
E3  9  1  4  1  -2
.ENDS MTH5N100
L7  8  9  100MH
RL  9  4  10
RPW 7  10  47
CBAT  10  4  10000UF     IC=200V
RBAT  9   10  0.1
VPW  10  8  PULSE(0  10  0  .1MS  .1MS  0.8MS  2MS)
.OPT  ITL5=0  RELTOL=.01
.TRAN  1M  60M  2M  UIC
.PROBE
.END
```

A.6 Static Characteristics of MPT3055

```
* THE CIRCUIT TO TEST THE STATIC CHARACTERISTICS OF A VDMOS
.OPTIONS ITL5=0 RELTOL=.01
XST  2  1  0  MTP3055E
VGS  1  0   1V
VDS  3  0   1V
VT   3   2  0V
.DC LIN VDS 0V  100V  .2V   VGS 4V  5V  .5V
.PROBE
.SUBCKT  MTP3055E  20  10  30
RG  10  1  10
M1  2  1  3  3  DMOS  L=1U  W=1U
.MODEL  DMOS  NMOS  (VTO=3.32 KP=5.5  THETA=.058 VMAX=1.4E5 LEVEL=3)
CGS  1  3  300P
RD  20  4  0.089
DDS  3  4  DDS
.MODEL  DDS  D (M=0.42 CJO=608.1P VJ=0.60)
DBODY  3  20  DBODY
.MODEL  DBODY D (BV=60  IS=1.1E-11  N=1.03 RS=0.50 TT=200N)
RA  4  2  1E-3
RS  3  5  1M
LS  5  30 5N
M2  1  8  6  6  INTER
E2  8  6  4  1  2
.MODEL INTER NMOS (VTO=0 KP=10 LEVEL=1)
```

```
CGDMAX  7  4  605P
RSGD  7  4  1E7
DGD  6  4  DGD
RDGD  4  6  1E7
.MODEL DGD  D (M=0.53 CJO=605P VJ=0.08)
M3  7  9  1  1  INTER
E3  9  1  4  1  -2
.ENDS
.END
```

A.7 Dynamic Characteristics of MTH5N100: Applying PWL at the Input

```
* THE CIRCUIT TO TEST A VDMOS, APPLYING A PWL WAVE AND GATE TO SOURCE RESISTAN
.OPTIONS ITL5=0 RELTOL=.01
XST  2  1  0  MTH5N100
VGS  4  0   PWL (0 0V 10NS 0V 46NS 20V 1.046US 20V 1.090US 0V)
VDD  3  0   170V
RG   1  4   100
RS   1  0   100
RL   2  3   20
.TRAN  1NS 4US
.PROBE
.SUBCKT  MTH5N100  20  10  30
RG  10  1  5
M1  2  1  3  3  DMOS  L=1U  W=1U
.MODEL  DMOS  NMOS  (VTO=3.36 KP=3.73 LEVEL=1)
CGS  1  3  1642P
RD  20  4  1.27
DDS  3  4  DDS
.MODEL  DDS  D (BV=1000 M=0.48 CJO=873P VJ=0.43)
DBODY  3  20  DBODY
.MODEL  DBODY D (BV=1000  IS=3.6E-11  N=1.03 RS=0.57 TT=1U)
RA  4  2  1E-3
RS  3  5  1M
LS  5  30 8N
```

```
M2  1  8  6  6  INTER
E2  8  6  4  1  2
.MODEL INTER NMOS (VTO=0 KP=10 LEVEL=1)
CGDMAX  7  4  7500P
RSGD  7  4  1E7
DGD  6  4  DGD
RDGD  4  6  1E7
.MODEL DGD  D (M=0.5 CJO=7500P VJ=0.00337)
M3  7  9  1  1  INTER
E3  9  1  4  1  -2
.ENDS
.END
```

A.8 Switching With Inductive Load

```
* THE CIRCUIT TO TEST A VDMOS, APPLYING A PWL WAVE AND GATE TO SOURCE RESISTAN
.OPTIONS ITL5=0 RELTOL=.01
XST  2  1  0  MTH5N100
VGS  4  0   PWL (0 0V 10NS 0V 46NS 20V 1.046US 20V 1.090US 0V)
VDD  3  0   170V
RG   1  4   100
RS   1  0   100
L   2  3   1MH
.TRAN  1NS 4US
.PROBE
.SUBCKT  MTH5N100  20  10  30
RG  10  1  5
M1  2  1  3  3  DMOS  L=1U  W=1U
.MODEL  DMOS  NMOS  (VTO=3.36 KP=3.73 LEVEL=1)
CGS  1  3  1642P
RD  20  4  1.27
DDS  3  4  DDS
.MODEL  DDS  D (BV=1000 M=0.48 CJO=873P VJ=0.43)
DBODY  3  20  DBODY
.MODEL  DBODY D (BV=1000  IS=3.6E-11  N=1.03 RS=0.57 TT=1U)
RA  4  2  1E-3
RS  3  5  1M
LS  5  30 8N
M2  1  8  6  6  INTER
```

```
E2  8  6  4  1  2
.MODEL INTER NMOS (VTO=0 KP=10 LEVEL=1)
CGDMAX  7  4  7500P
RSGD  7  4  1E7
DGD  6  4  DGD
RDGD  4  6  1E7
.MODEL DGD  D (M=0.5 CJO=7500P VJ=0.00337)
M3  7  9  1  1  INTER
E3  9  1  4  1  -2
.ENDS
.END

* THE CIRCUIT TO TEST A VDMOS, APPLYING A PWL WAVE AND GATE TO SOURCE RESISTAN
.OPTIONS ITL5=0 RELTOL=.01
XST  2  1  0  MTH5N100
VGS  4  0   PWL (0 0V 10NS 0V 46NS 20V 1.046US 20V 1.090US 0V)
VDD  3  0   170V
RG   1  4   100
RS   1  0   100
L   2  3   1MH
.TRAN  1NS 4US
.PROBE
.SUBCKT  MTH5N100  20  10  30
RG  10  1  5
M1  2  1  3  3  DMOS  L=1U  W=1U
.MODEL  DMOS  NMOS  (VTO=3.36 KP=3.73 LEVEL=1)
CGS  1  3  1642P
```

```
RD  20  4  1.27
DDS  3  4  DDS
.MODEL  DDS  D (BV=1000 M=0.48 CJO=873P VJ=0.43)
DBODY  3  20  DBODY
.MODEL  DBODY D (BV=1000  IS=3.6E-11  M=1.03 RS=0.57 TT=1U)
RA  4  2  1E-3
RS  3  5  1M
LS  5  30 8N
M2  1  8  6  6  INTER
E2  8  6  4  1  2
.MODEL INTER NMOS (VTO=0 KP=10 LEVEL=1)
CGDMAX  7  4  7500P
RSGD  7  4  1E7
DGD  6  4  DGD
RDGD  4  6  1E7
.MODEL DGD  D (M=0.5 CJO=7500P VJ=0.00337)
M3  7  9  1  1  INTER
E3  9  1  4  1  -2
.ENDS
.END
```

Appendix B

Program Listings For LUT

B.1 Assembly Language Program For Digital Feedback

```
;this program will open file tst.tmp
;read the value of the output voltage and then
;perform pulse width calculation
;file tst.tmp will be read
;initial conditions will be read
;these intial condtions will be put in cmdt.cir for the next run
;the new calculated value for pwm will also be put in cmdt.cir

code segment
assume  cs:code,ds:code
org 100h
first: jmp main

tmp db 'c:\prospice\tst.tmp0' ;address of temp file
new db 100 dup(?) ;the temp file is read and stored here
pwmp db 'c:\prospice\pwm.ptr0'  ;address of pwm.ptr file
new1 db 10 dup(?)          ;the ptr file is read and stored here
minus db 0 ;store the minus sign
savedx dw ?

file proc near
lea dx,tmp ;proc for opening file
mov ax,seg tmp ;and reading bytes
```

```
mov ds,ax
mov al,0
mov ah,3dh ;open file tst.tmp for reading
int 21h
lea dx,new
mov cx,100d
mov bx,ax ;read 100 bytes
mov ah,3fh ;put the bytes read in location 'new'
int 21h
ret
file  endp


asc2h  proc near
push bx
push cx
push dx ;save the registers
push si
lea dx,new+15 ;load the address of string
mov bl,[new+22]
sub ax,ax
cmp bl,'-' ;convert the decimal of the string
je exit
mov bl,[new+24] ;see the exponent portion
cmp bl,30h
je ski
```

```
inc bl
ski: inc bl
inc bl
and bx,0fh ;convert to binary
mov cx,bx ;characters in the string
cld ;make string instruction go forward
mov si,dx ;read the string
mov al,[si] ;first character
cmp al,'-' ;is it a minus sign
jne decs1
mov minus,1 ;put 1 in the location minus
jmp decs1 ;go adjust the count and pointer

decs1: dec cx
inc si

clrdx: sub dx,dx
nxtchr: call dxtms10
skp: lodsb ;read the next string character
cmp al,'0'
jb pnad
cmp al,'9' ;see if the character is numeric
ja  pnad
and ax,0fh ;convert it to binary
  add dx,ax
loop nxtchr ;repeat until count is over
```

```
mov ax,dx
cmp minus,1
jne exit ;see if the string was negative
neg ax ;yes negate ax
jmp exit ;and then leave
pnad: cmp cx,1
je skp
dec cx
jmp skp ;dec the counter
exit: pop si
pop dx
pop cx ;restore the register and return
pop bx
ret
asc2h endp

dxtms10 proc near
mov savedx,dx
shl dx,1
shl dx,1    ;proc to multiply contents of dx by 10
add dx,savedx
shl dx,1
ret
dxtms10 endp

pwm proc near
```

```
lea dx,pwmp ;proc for opening file
mov ax,seg pwmp ;and reading bytes
mov ds,ax
mov al,0
mov ah,3dh ;open file pwm.ptr for reading
int 21h
lea dx,new1
mov cx,100d
mov bx,ax ;read 10 bytes
mov ah,3fh ;put the bytes read in location 'new1'
int 21h
mov al,new1

ret
pwm endp

main proc near
call  pwm ;calls proc to read pwm.pnt
call  file ;calls proc to read *.tmp
call  asc2h ;call ascii to binary procedure
main endp
;*******************************************************************************
        mov   ah,4ch
 int 21h
code ends
        end   first
```

B.2 Turbo Basic Program to Provide Digital Feedback

```
a% = 0
b% = 0
c% = 0
dta$ = ""
ics$ = ""
ptr$ = ""
tmp$ = ""
eta$ = ""
open "pwm.ptr" for binary as #1
seek #1, 1     'start from the first byte
get$ 1, 4, ptr$  'read the value from file pwm.ptr
seek #1, 8
get$ 1, 4, tbl$
seek #1, 15
get$ 1, 4, cnt$
close #1
print "read values ptr, tbl, cnt",ptr$,tbl$,cnt$
a% = val(ptr$)  'holds the value of  pointer
t% = val(tbl$)          'table of the modulation index
x% = val(cnt$)               'decision making value

'*************************************************************
```

```
if x% < 32 then          'check whether it is first quadrant
 e% =  (t% * 40) + a%
 a% = a% + 8
 print "it is first quad", a%

elseif x% = 32 then
 e% = (t% *40) + a%     'see whether the top of wave reached
 a% = a% + 8
 goto fback

elseif x% < 80 and x% >= 40  then  'check whether it is in sec quadrant
 a% = a% - 8
 e% = (t% * 40) + a%
 print "it is in second quad",a%

elseif x% < 120 and x% >= 80  then 'check whether it is in third quad
 e% = (t% * 40) + a%
 a% = a% + 8
 print "it is third quad",a%

elseif x% < 160 and x% >= 120  then 'check whether it is in fourth quad
 a% = a% - 8
 e% = (t% * 40) + a%
 print "it is fourth quad",a%

end if
```

```
'*******************************************************
goto ptr

 fback:

 open "tst.tmp" for binary as #2
 seek #2,15 'read from the 16 byte
 get$ #2, 10, tmp$        'upto 25 byte
 close #2
 b% = val(tmp$)
 print "this is voltage o/p at 1/4 and feed back taking place";b%


if b% > 100 and b% < 120  then 'check if the value of voltage within range
 goto ptr
  elseif b% < 100 then
  t% = t% + 2        'take higher modulation index
   elseif b% > 120 then
   t% = t% - 2        'take lower modulation index
 print " modulation index changing", t%
end if

ptr:   'put the required enteries in *.cir and pwm.ptr
open  "lut.dta"  for binary as #3  'open look up table
open  "tst.tmp"  for binary as #2  'open the tmp file
```

```
seek #2, 15
get$ #2, 10, tmp$  'read the capacitor voltage
seek #2, 27
get$ #2, 10, ic$ 'read the inductor current from tst.tmp
close #2
seek #3, e%   'read the value from table pointed to by e%
get$ #3, 6, dta$  'data string is dta$
close #3
c# = 0
print "table value dta$ ",dta$
c# = val(dta$)
print "this is C#", c#

if x% >= 80 then
 c# = 1000 - (c#)
 dta$ = str$(c#)
 dta$ = left$(dta$,6)
 print "third and fourth quad ",dta$
end if

m# = (c#) + (0.3)
eta$ = str$(m#)   'after adding 200ns convert back to ascii string form
eta$ = left$(eta$,6)
print "modified value eta$ ",eta$ 'the value of data read from the table
```

```
open  "cmfb3.cir" for binary as #4 'open the circuit file
seek #4, 59
put$ #4, "0000.0"  'this is just to make sure that blank is taken care of
seek #4, 59
put$ #4, dta$   'put the pwl time
seek #4, 70 'put the pwl sec time
put$ #4, "0000.0"
seek #4, 70
put$ #4, eta$
seek #4, 108
V$ = "V"
A$ = "A"
put$ #4, tmp$ + V$       'put the initial conditions for cap
seek #4, 144
put$ #4, ic$  + A$       'put the initial conditions for inductor
x% = x% + 8  'each entry occupies eight bytes

if x% >= 160 then
 x% = 0
end  if

'*************************************************************************
open "pwm.ptr" for binary as #1 'open the pointer file
ptr$ = str$(a%)
tbl$ = str$(t%)
cnt$ = str$(x%)
```

```
ptr$ = left$(ptr$,5)
tbl$ = left$(tbl$,5)
cnt$ = left$(cnt$,5)

print "written values ptr, tbl, cnt ",ptr$,tbl$,cnt$

for h% = 0 to 20
 seek #1, h%          'clear the previous enteries of the file
 put$ #1, chr$(32)
next h%

seek #1, 0
put$ #1, ptr$
seek #1, 7          'store a% , x%, and t% in pwm.ptr
put$ #1, tbl$
seek #1, 14
put$ #1, cnt$
close
end
```

B.3 A Program to Generate Look-Up Table Data

```
'open a file for sequential
open "lut.dta" for output as #1
Tc! = .001                          'pulse width in secconds
S! = .005                            'step size .005
for M% = 0 to 45
  for J% = 1 to 5
    Th! = Tc! / 2 * (1 + ( .75 + M% * S! ) * sin(314.1592 * ((Tc! / 4)  + (J% * Tc!
     Th! = Th! * 1000000
     b$ = str$(Th!)
     c$ = left$(b$,6)
    print #1, c$
  next J%
next M%
close# 1
end
```

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